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# A COMPARATIVE STUDY OF MACRO MODELS OF SINGLE ELECTRON TRANSISTOR

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***ABSTRACT:*** *Single Electron Transistor (SET) is a key element in research of nano scale devices. The single electron transistor can utilize in Ultra Large Scale Integration (ULSI) chip to reduce the power consumption. This paper includes different macro models used for simulation of single electron transistor. The macro model is an efficient method for simulation of single electron circuits. It also describes and compares the $I_{ds}$- $V_{ds}$ and $I_{ds}$- $V_{gs}$ characteristics of different macro models.*

***Keywords: Single electron transistor, Macro-model***

## I. INTRODUCTION

The single electron transistor is considered as one of the main candidates for the basic elements of future ULSI chips. Single-electron tunnelling devices utilize effects of quantized nature of charge. The single electron technology deals with the control of the transport of a single electron or a small number of electrons. The fundamental physical principles of single electronics are the tunnelling effect and the Coulomb blockade.

There have been lots of efforts for the development of single electron circuit simulators. In these simulators, Monte-Carlo methods are used for the probability calculation of the Coulomb island but a large amount of simulation time is needed. For efficient design and simulation of single electron circuits, a compact model would be required such as in the case of conventional circuit simulators (SPICE).

The SPICE macro model of the SET is an efficient method for simulation of single electron circuits. The macro model efficiently reproduces Monte-Carlo calculation results with a reasonable accuracy.

The Macro Model uses SPICE simulator to simulate the characteristics of SET circuits. In this simulator, two assumptions are used for model: (1) Once the parameter of the isolated transistor is determined from the device simulator, it can be used in whole circuit. I-V characteristic of the device is the function of the device width. (2) I-V characteristic of the device is affected by neighboring transistors only through the changes of the terminal voltages of the transistor.

## II. SET MACRO MODEL

The macro model for simulation of single electron transistor is shown in Fig 2. It consists resistor $R_G$ with a large resistance of 100GΩ connected between

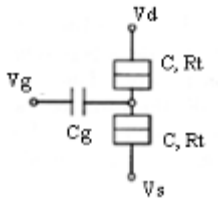


Figure 1 Equivalent circuit of SET [7]

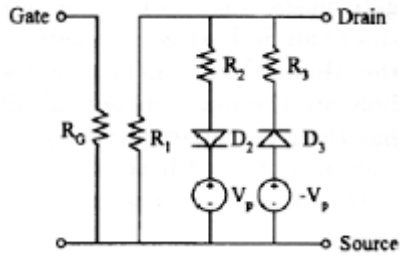


Figure 2 SET macro model proposed by Yu et al [7]

gate and source. Symmetric $I_{ds}$-$V_{ds}$ characteristic obtained with two branches consisting of resistors, diodes, and voltage sources are identical. The directions of $D_2$ and $V_2$ are opposite to those of $D_3$ and $V_3$ to have the flow of current in both positive and negative drain-source bias. $R_1$ is the primary resistor in coulomb blockade region. $R_2$ and $R_3$ are resistors of SET in non-coulomb blockade region when its $V_{ds}$ is larger than a certain value in positive

and negative direction, respectively. The charging energy periodically changing as a function of the gate bias is included in $R_1$, $R_2$ and $R_3$ as the cosine of the gate bias. They are expressed as follows [7];

$$R_1(V_G) = CR_1 + CR_2 . \cos(CF_1 . V_G)$$
$$R_2(V_G) = R_3(V_G) = \frac{CV_p}{CI_2 - \frac{2CV_p}{R_1(V_G)}}$$

Where, $CF_1$, $CV_p$, $CI_2$, $CR_1$ and $CR_2$ are used as the fitting parameters for the current-voltage characteristics at different gate biases. The SET has the gate capacitance Cg = 3.2aF, the junction capacitance C = 1.6aF, the tunnel resistance $R_t$ = 100 MΩ, and the temperature T = 30 K. The macro model parameters are determined by fitting the Monte-Carlo result with piecewise linear approximation. The macro model parameters are the functions of T.

The parameter values,
$CF_1 = 60$
$CV_p = 0.02$
$CI_2 = 0.2 * 10^{-9}$
$CR_1 = 300 * 10^6$
$CR_2 = 100 * 10^6$

In the model of Yu et al., the drain-source current, Ids, increases linearly with the drain-source voltage, $V_{ds}$ in the Coulomb blockade region. For practical SETs, the Ids should change exponentially with $V_{ds}$ in the Coulomb blockade region.

Fig 3 shows macro model proposed by Wu and Lin. In which, two face-to-face ideal diodes $D_4$ and $D_5$ are connected instead of a large resistor $R_G$, to block all possible current flows from gate to source in the SET.

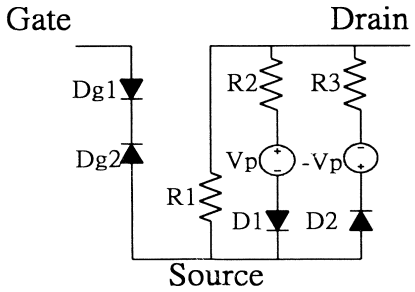


Figure 3 SET macro model proposed by Wu and Lin [8]

The Ids should be exponential function of $V_{ds}$ due to tunnelling of electron through the tunnelling junction, for that $R_1$, $R_2$ and $R_3$ have to be a function of $V_{ds}$ as well and are modified as follows [8]:

$$R_1(V_G, V_{ds}) = CR_1 + CR_2[\cos(CF . \pi . V_G) + 1] . 2^{(CV_p - V_{ds}x)}$$

$$R_2(V_G, V_{ds}) = R_3(V_G, V_{ds}) = \frac{CV_p}{CI_2 - \frac{2CV_p}{R_1(V_G, V_{ds})}}$$

where x is a function of temperature.
The expression for $CR_1$, $CR_2$, CF and $CV_p$ are:
$CR_1 = 4R_j$
$CR_2 = 1.33R_j$
$CF = 2C_g / e$
$CV_p = 0.02$

Here $R_j$ is the junction tunnelling resistance and Cg gate normal capacitance.

However, in above two models, SET devices are described by the orthodox theory. In this theory, the time needed for the tunnel event is assumed to be zero. Therefore, to get a more accurate model that includes the electron tunnelling time, Mohammad Pouyan and Rahim Faez proposed a new macro-model.

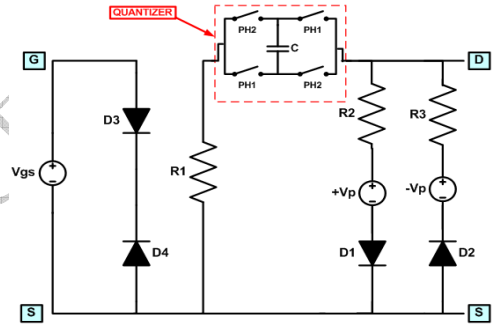


Figure 4 SET Macro-model with quantizer block [9]

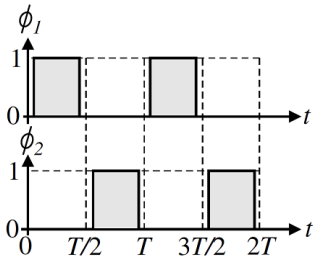


Figure 5 Two-phase, non-overlapping clock [9]

The function of the SET is based on the Coulomb blockade theory, which is a consequence of the discreteness of the electron charge.

When an electron is added to the metallic island, this will create a difference in charge between the island and its environment, meaning that the capacitor between the island and the environment will be charged with a charge e. The energy required to increase the charge on the capacitor of the central island by one electron, which is $E_c = e^2/2C >> K_BT$, can be quite significant. To travel from the source to

the drain, electrons must overcome this charging energy barrier.

In the orthodox theory, the time needed for the tunnel event is assumed to be zero. In a real situation, the main quantum property of the SET device is the phenomenon of electron tunnelling and the time needed for the tunnel event is important, especially in complicated circuits, for delay time calculation. This model explores the discrete character of the tunnel current and in contrast to the prescriptions, the tunnelling time is not equal to zero in this model, and it can be evaluated.

The circuit including SET junctions can be described by a discrete charge transfer through the tunnel junctions. During this discrete charge transfer, the tunnel event is modelled as a quantizer block to obtain a quantified output signal on the island, which allows the tunnelling-time calculation. This block consists of a bilinear-switched capacitor-resistor emulation circuit. In other words, the charge redistribution quantizer is a switched capacitor circuit, where the charge stored on a capacitor is used to perform the quantization.

The bilinear-switched capacitor-resistor emulation circuit, quantizer block consists of four controlled switches and a capacitor, C. The switches are controlled by using the clock waveforms. There are two non-overlapping clock waveforms, Φ1 and Φ2, each one controlling two switches at the same time. The period of the clock waveforms is T, and the width of each individual clock is slightly less than T/2, as shown in Fig. 5. The bilinear-switched capacitor circuit is equivalent to a resistor if the changes in the input and the output of the circuit can be neglected during the period T. On this condition, the equivalent resistance of the bilinear switched capacitor-resistor circuit is T/4C.

It is noted that Ids should be exponentially dependent on $V_{ds}$ due to the tunnelling of electrons through the tunnelling junction. To account the Ids as a exponential function of $V_{ds}$ inside the Coulomb blockade region, $R_1$, $R_2$ and $R_3$ have to be functions of $V_{ds}$ as well. As shown in Fig. 4, $R_1$ is in series with the equivalent resistance of the bilinear-switched capacitor circuit, $CR_1$ = T/4C. To achieve the best compatibility, we have modified all resistors equations in our model as follows [9]:

$$R_1(V_G, V_{ds}) = CR_2\,[\cos(CF.\pi.V_G) + y].\ 2^{(CV_p - V_{ds}.x)}$$

$$R_2(V_G, V_{ds}) = R_3(V_G, V_{ds}) = \frac{CV_p}{CI_2 - \frac{2CV_p}{R_1(V_G, V_{ds}) + CR_1}}$$

The switched capacitor equivalent resistance is given by $T_{sw}$/4C

$CR_1 = T_{sw}/4C$
$CR_2 = 1.33R_j$ (For T = 30 K)
$CF = 2C_g/e$
$CV_p = 0.02$

Here, y is a positive parameter and a function of $V_{ds}$, x is a function of temperature, $R_j$ is the junction tunnelling resistance, $C_g$ is the gate normal capacitance, $T_{sw}$ is the period of the clock waveforms in the switched capacitor circuit. $CR_1$ and $CR_2$ are temperature-dependent parameters as specified in the model of Yu et al. The capacitance C in the switched capacitor circuit depends on the quantity $CR_1$ at the specified temperature.

## III. SIMULATION RESULTS

Fig. 6 shows the $I_{ds}$-$V_{ds}$ characteristics obtained from Yu et al's model, for both the Coulomb blockade and the non-Coulomb blockade regions. Fig. 7 shows the $I_{ds}$-$V_{ds}$ characteristics obtained from Yu et al's model, for the Coulomb blockade region in positive direction only.

The presence of the Coulomb blockade in the $I_{ds}$-$V_{ds}$ characteristics of the SET is a region of zero current for a range of small drain-source voltage biases. The drain-source current $I_{ds}$ is a linear function of drain-source voltage $I_{ds}$.

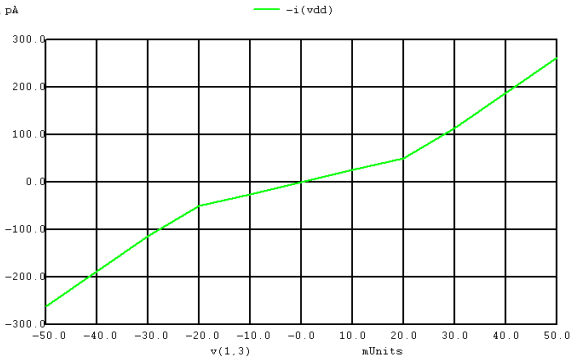


Figure 6 $I_{ds}$-$V_{ds}$ characteristic, Yu et al's model

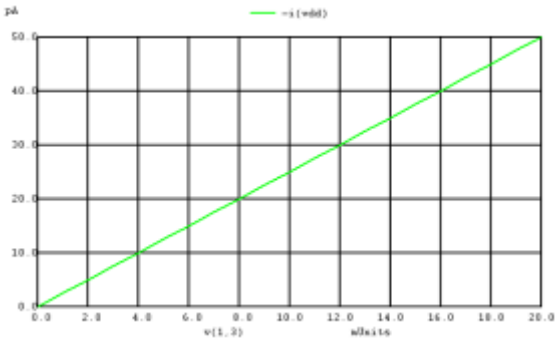


Figure 7 $I_{ds}$-$V_{ds}$ characteristic in coulomb blockade region, Yu et al's model

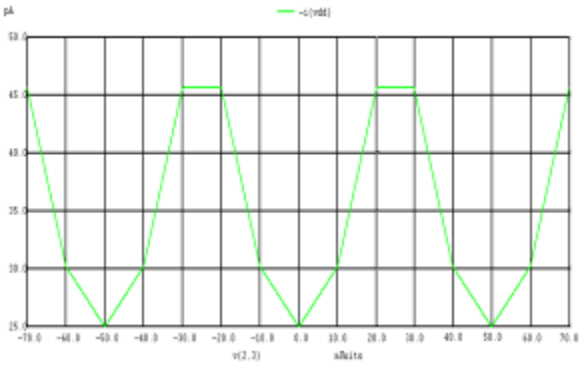

Figure 8 $I_{ds}$-$V_{gs}$ characteristic, Yu et al's model

The current flowing from the source to the drain in a SET depends on the tunnelling probability through both the drain-tunnelling junction and the source tunnelling junction.

Fig 8 shows the $I_{ds}$-$V_{gs}$ characteristic obtained from Yu et al's model. Coulomb oscillations of Ids as a function of $V_{gs}$ are observed due to capacitively coupled tunnel junction and Coulomb Island. The current flowing between gate and source was added to $I_{ds}$.

In an ideal SET, the isolation between the gate and Coulomb Island makes the current flowing from gate to source negligibly small.

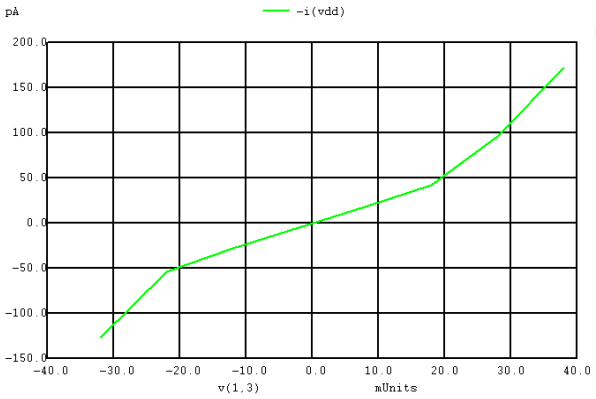


Figure 9 $I_{ds}$- $V_{ds}$ characteristic, Wu and Lin model

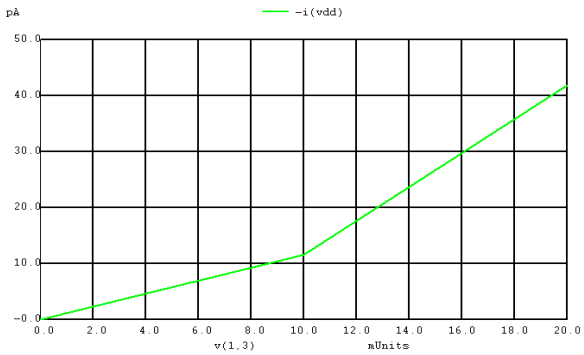


Figure 10 $I_{ds}$- $V_{ds}$ characteristic in coulomb blockade region, Wu and Lin model

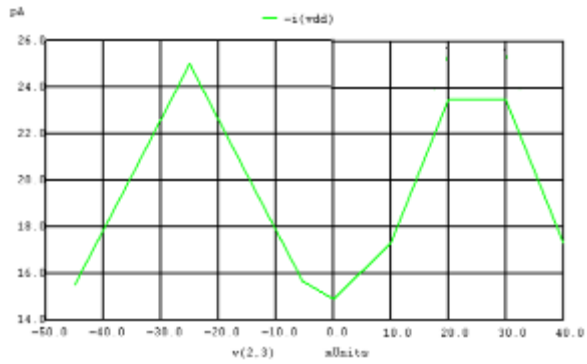


Figure 11 $I_{ds}$- $V_{gs}$ characteristic, Wu and Lin model

Fig 9 shows the $I_{ds}$- $V_{ds}$ characteristic obtained from Wu and Lin model for both coulomb blockade and non-coulomb regions. Fig 10 shows the $I_{ds}$-$V_{ds}$ characteristic for coulomb blockade region for $R_j$ = 100MΩ, $C_j$ = 1.6aF, $C_g$ = 3.2aF, and T = 30 K.

In an ideal SET, the drain-source current Ids should be an exponential function of drain-source voltage $V_{ds}$. Wu and Lin model gives exponential function for $I_{ds}$- $V_{ds}$ at some level shows in Fig 10.

Fig 11 shows the simulation result of $I_{ds}$- $V_{gs}$ characteristic obtained from Wu and Lin model. The coulomb oscillation is seen from this figure.

Here, the current flowing between gate and source reduced to almost 50% as compared to Yu et al's model.

Fig 12 shows the $I_{ds}$- $V_{ds}$ characteristic obtained from Mohammad Reza Karimian and Massoud Dousti model for both the Coulomb blockade and the non-Coulomb blockade regions. This model gives the coulomb blockade region equal to $CV_p$.

The drain-source current Ids should be an exponential function of drain-source voltage $V_{ds}$, which is clearly shown in Fig 13 for $R_j$= 100 MΩ, $C_j$ = 1.6 aF, $C_g$ = 3.2 aF, and T = 30 K.

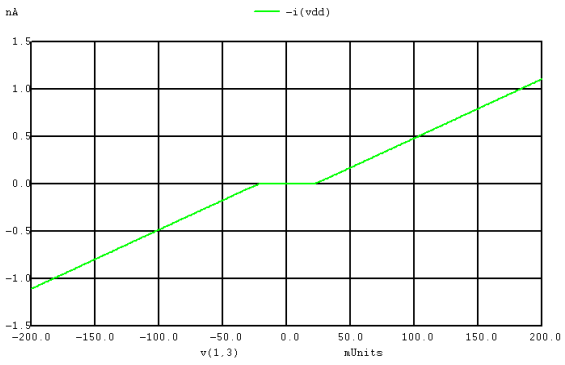


Figure 12 $I_{ds}$- $V_{ds}$ characteristic, Karimian and Dousti model

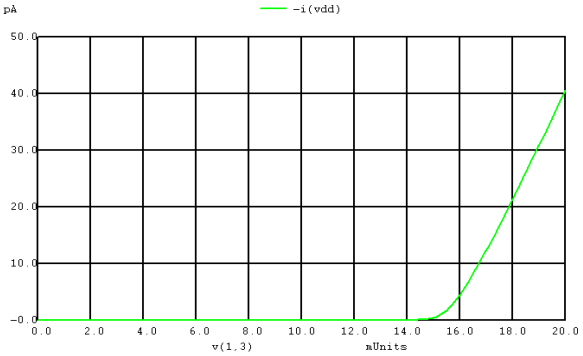


Figure 13 $I_{ds}$- $V_{ds}$ characteristic in coulomb blockade region, Karimian and Dousti model

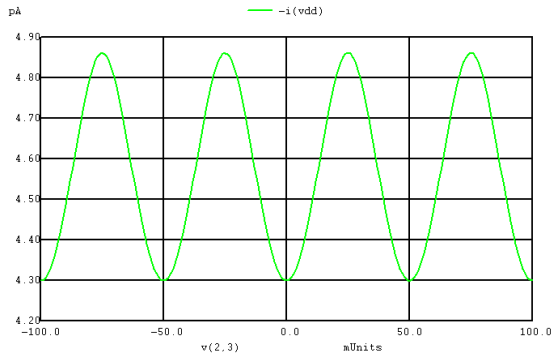


Figure 14 $I_{ds}$- $V_{gs}$ characteristic, Karimian and Dousti model

Fig 14 reveals the simulated $I_{ds}$- $V_{gs}$ characteristics of SET that obtained from Mohammad Reza Karimian and Massoud Dousti model at T=30K. The Coulomb oscillation can be clearly seen from this figure. The current flowing between gate and source reduced considerably.

## IV. CONCLUSION

Macro model proposed by Yu et al gives linear function of $I_{ds}$ w.r.t $V_{ds}$. Coulomb oscillations of Ids as a function of $V_{gs}$ are also observed. Macro model proposed by Wu and Lin, gives exponential function for $I_{ds}$- $V_{ds}$ characteristic. In this model, the current flowing between gate and source reduced to almost 50% as compared to Yu et al's model. Macro model proposed by Mohammad Reza Karimian and Massoud Dousti, gives $I_{ds}$ is an exponential function of $V_{ds}$. The current flowing between gate and source reduced more and calculate tunnelling time.

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