

DESIGN AND IMPLEMENTATION OF I2C BUS CONTROLLER USING VERILOG

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ABSTRACT: The I2C protocol was given by Philips Semiconductors in order to allow faster devices to communicate with slower devices and also allow devices to communicate with each other over a serial data bus without data loss. I2C enabled microcontrollers like PIC18F452 from Atmel and TMS470 from Texas Instruments requires a lot of programming and knowledge of the register structures for configuring it. Hence they are not portable. We here present a model of I2C bus controller. The I2C controller is designed using verilog in xilinx 11.1 and targeted in virtex 4 and virtex 5.

Index Terms — I2C Bus, master, slave, verilog, Finite state machine

I. INTRODUCTION

The EEPROM, ADC and RTC will require an interface for communication between them. So I2C bus is used as an interface between them. It is used to minimize system-level interconnect. This simplifies the system level design and the design of the motherboard and associated chip-boards. Moreover transmitting information over the I2C bus will improve system performance since the transmission of digital data is much less susceptible to interference from environmental noise sources.

II. I2C BUS SPECIFICATIONS

The I2C Controller Bus is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. I2C provides good support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. I2C is easy to use to link multiple devices together since it has a built-in address [1][2]. The two I2C signals are serial data (SDA) and serial Clock (SCL) as shown in Figure 1. The device that initiates a transaction on the I2C bus is termed the master. The master normally controls the clock signal. A device being addressed by the master is called a slave [1][2].

The I2C protocol supports multiple masters, but most system designs include only one. There may be one or more slaves on the bus. Both masters and slaves can receive and transmit data bytes. Standard I2C devices operate up to 100Kbps, while fast-mode devices operate at up to 400Kbps. Most of the I2C devices available today support 400Kbps operation. Higher-speed operation may allow I2C to keep up with the

rising demand for bandwidth in multimedia and other applications[2].

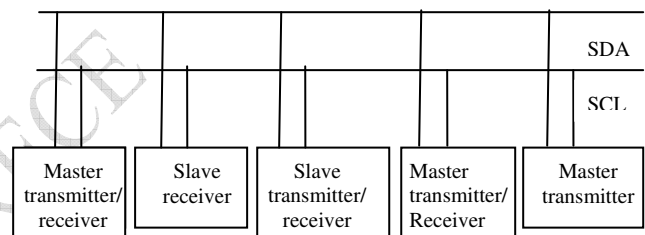


Fig. 1 I2C bus configuration using masters and slaves

III. I2C CHARACTERISTICS

The SDA and SCL lines are bi-directional lines connected to a positive voltage supply through a pull-up resistor. The bus is free when these lines are 'high'. The data on the SDA line is valid only when the SCL line is 'high'. Change of data is allowed when SCL line becomes 'low'. During data transfer, the master generates the START and STOP conditions, which are unique conditions and are shown in Figure[2].

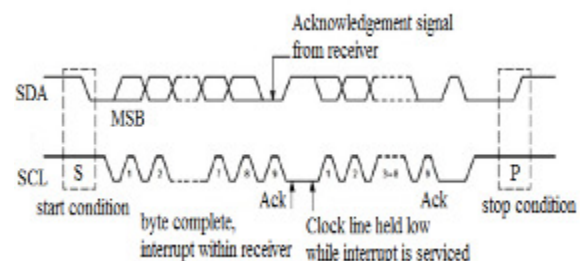


Fig. 3 Data transfer on the I2C bus

IV. I2C BUS CONTROLLER DESIGN

I2C protocol consists of four parts 1) START signal generation, 2) Slave address transfer, 3) Data transfer, 4) STOP signal generation [12].

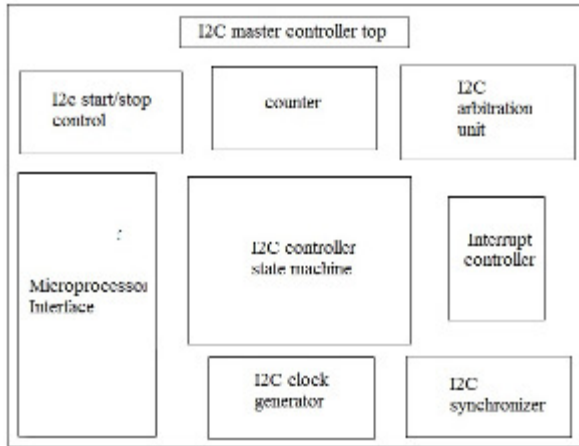


Fig. 4 The I2C Master Controller Block Diagram

V. I2C BUS ARCHITECTURE

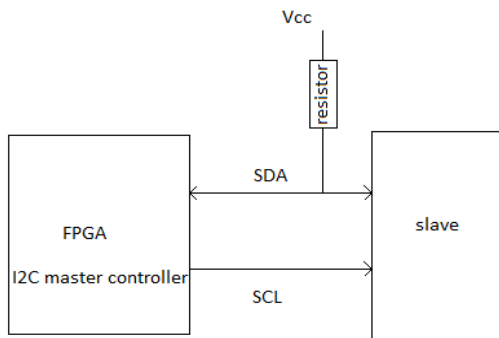


Fig. 5.1 I2C bus architecture

It consists of a master and a slave connected using I2C bus. The SDA line is connected to a positive supply voltage through a pull up resistor. The SCL line is not connected to a pull up resistor as there is only one master.

Designing the I2C master controller

For designing the I2C master controller is to use a finite state machine (FSM). We can easily implement finite state machine by writing VHDL or verilog code [15].

Finite State machine

A finite state machine is a sequential circuit that uses a finite number of states to keep track of its history of operations, and based on this history and its current inputs, determine what to do next.

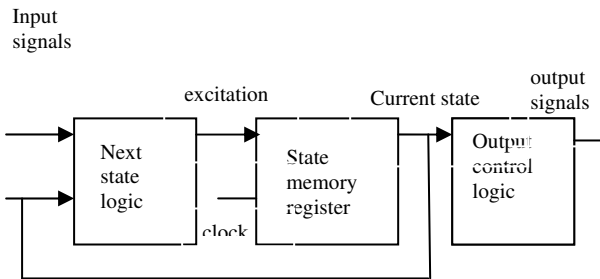


Figure 5.2 Block diagram of finite state machine

A sequential circuit is one where its outputs are dependent on its history of operation and its current inputs.

VI. RESULT ANALYSIS

Here the I2C bus controller is designed using verilog and implemented in virtex 4 xc4vlx15-12sf363 using xilinx 11.1. The device utilization summary is given below:

Device utilization summary(virtex 4)			
Logic utilization	Used	Available	Utilization
Number of slices	44	6144	0%
Number of slice flipflops	52	12288	0%
Number of 4 input LUTs	81	12288	0%
Number of bonded IOBs	18	240	7%
Number of GCLKs	1	32	3%

Here the I2C bus controller is designed using verilog and implemented in virtex 5 xc4vlx15-12sf363 using xilinx 11.1. The device utilization summary is given below:

Device utilization summary(virtex 5)			
Logic utilization	Used	Available	Utilization
Number of slices	52	19200	0%
Number of slice flipflops	63	19200	0%
Number of 4 input LUTs	46	69	66%
Number of bonded IOBs	18	220	8%
Number of GCLKs	1	32	3%

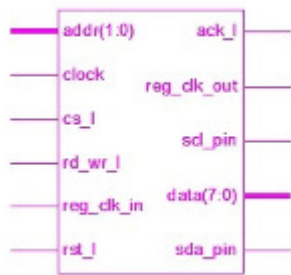


Figure 6.1 RTL view

VII. CONCLUSION

The result shows that minimal resources are utilized in virtex 4. The design process is simplified using verilog HDL to design the I2C bus controller. The designer can write his design description without choosing any specific fabrication technology. If a new technology emerges, designers do not need to redesign the circuit. He simply input the design program to the logic synthesis tool and creates a new gate level netlist using the new fabrication technology. The logic synthesis tool will optimize the circuit in area and timing for the new technology.

VIII. REFERENCES:

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