

Design and Implementation OF Logic-BIST Architecture for I2C Slave VLSI ASIC Design Using Verilog

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ABSTRACT: Built-in self-test for logic circuits or logic BIST, is an effective solution for the test cost, test quality, and test reuse problems. Logic BIST implements most ATE functions on chip so that the test cost can be reduced through less test time, less tester memory requirement, or a cheaper tester. Logic BIST applies a large number of test patterns so that more defects, either modeled or un-modeled, can be detected. IN addition, logic BIST makes it easy to conduct the at-speed test for detecting timing-related defects. Furthermore, a BISTed-core makes SoC testing easier. Most of logic BIST schemes are based on the STUMPS structure, which applies random patterns generated by a PRPG to a full-scan circuit in parallel and compresses the responses into a signature with a MISR. This signature is compared with Golden signature to check test pass/fail information and defect or not. Expected output includes the Designed STUMP Based Architecture, Which is Test per Scan Using Verilog HDL and Simulation Result having information of design is defect free or not.

KEY WORDS: BIST, DFT, DUT, Fault Coverage, LFSR, MISR, Scan Test, Seed, Signature, STUMPS.

I. Introduction

Testing of integrated circuits (ICs) is of crucial importance to ensure a high level of quality in product functionality in both commercially and privately produced products. The impact of testing affects areas of manufacturing as well as those involved in design. Given this range of design involvement, how to go about best achieving a high level of confidence in IC operation is a major concern. This desire to attain a high quality level must be tempered with the cost and time involved in this process. These two design considerations are at constant odds. It is with both goals in mind (effectiveness vs. cost/time) that Built-In-Self Test (BIST) has become a major design consideration in Design-For-Testability (DFT) methods.

II. PROBLEM OF VLSI TESTING

- Need for a cost-efficient testing
- Long test-pattern generation and test application times
- Prohibitive amounts of test data must be stored in the ATE
- Chip/Board Area Cost vs. Tester Cost
- Diagnosis and repair time
- Maintenance test requires the presence of an expensive ATE at the site of the failing system with significant cost
- At-speed testing using External ATE
- There is a lack of skilled test engineers

III. BENEFITS OF BIST

- Reduces testing and maintenance cost
- Reduces cost of automatic test pattern generation (ATPG).
- Reduces storage and maintenance of test patterns.
- Can test many units in parallel.
- Takes shorter test application times.
- can test at functional system speed

IV. BIST Architecture

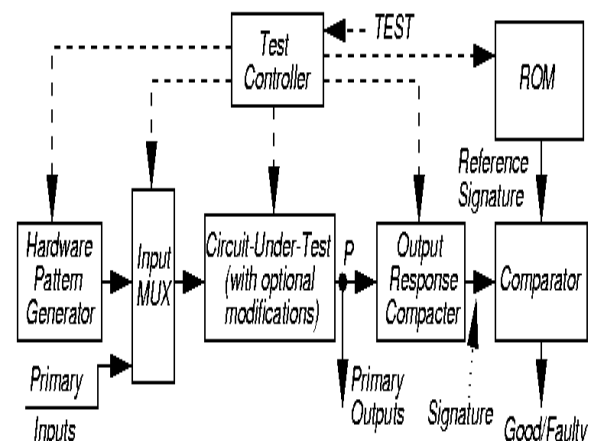


Fig. 1 General BIST Architecture

On a very basic level, BIST needs a stimulus (the Test Pattern Generator (TPG) in this case), a circuit to be tested, a way to analyze the results, and a way to compress those results for simplicity and handling.

However, BIST designs can differ in many ways. Each method has its own set of trade-offs and design considerations. If the BIST design is not appropriate for the IC it is testing, then it can actually be a detriment to the design. The components that the logic BIST is comprised of pseudo-random pattern generator (PRPG) and the phase shifter circuit. The output response analysis block -composed of multiple input signature register (MISR) and the signature analyzer.

V. STUMPS Based Architecture

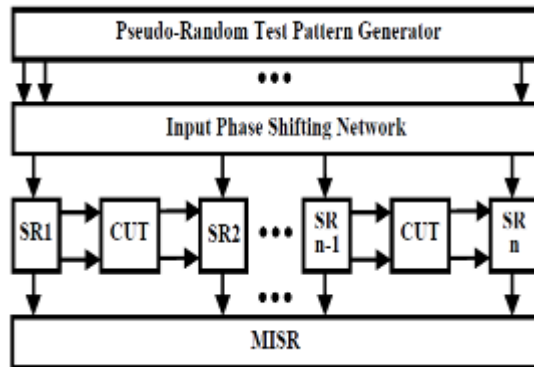


Fig. 2 STUMPS Architecture

The most widely used BIST in industry today is self-testing using MISR and PRPG (SRSG) (STUMPS). This BIST architecture solves the problem of long internal scan chain of a CUT (as in RTS and LOCST) by splitting the internal scan into several individually accessible scan chains. Preferably, the scan chains should be of equal or close lengths, but there is no penalty if this is not done. Figure 2 shows a generic form for the application of STUMPS BIST method to the Huffman model of our CUT. As shown three separate scan chains are used here. The serial input of each scan chain is driven by a bit of the parallel output of a PRPG. This result in pseudo-random serial test data shifted into the scan chain. The serial outputs of the internal CUT scan chains drive the bits of the parallel input of an MISR.

The architecture of the self-testing using MISR and parallel SRSG (STUMP) is shown in Figure. Instead of using only one scan chain, it uses multiple scan chains to minimize the test time. Since the scan chains may have different lengths, the LFSR runs for N cycles (the length of the longest scan chain) to load all the chains. For such a design, the internal type LFSR is preferred. If the external type is used, the difference between two LFSR output bits is only the time shift. Hence, the correlation between two scan chains can be very high.

A. STUMPS Test Process

1. Scan in patterns from LFSR to all scan chain.
2. Switch to normal function mode and apply one clock.
3. Scan out chains into MISR.

4. Overlap steps 1 and 3.

B. BIST Implementation

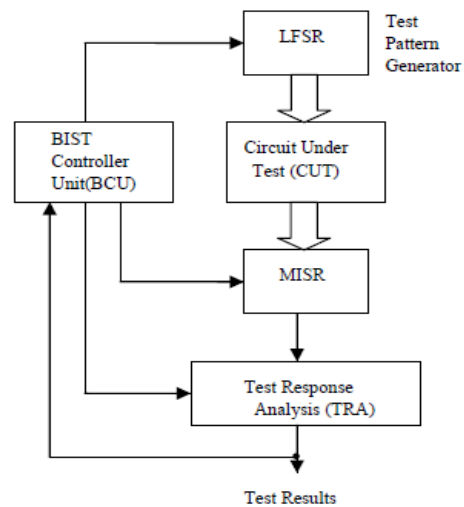


Fig. 3 BIST Implementation

VI. BIST COMPONENT AND OPERATION

A. LFSR (Linear Feedback Shift Register)

Data produced by an LFSR are based on what is referred to as its characteristic equation, which is defined by the way its feedback is formed. The Linear Feedback Shift Register, one of the main parts of BIST is a clocked synchronous shift register augmented with appropriate feedback Network and receiving Seed value and Polynomial as a input. The only signal necessary to generate the test patterns is the clock. The random numbers generated are used to identify the physical faults in the IC. It is a sequential shift register with combinational logic and it pseudo randomly cycle through a sequence of binary values. Feedback around an LFSR's shift register comes from a Polynomial in the register chain and constitutes XORing these taps to provide tap(s) back into the register.

A parameter based Generalized LFSR has been designed for this project. It is because in this programmable LFSR when we give the size as input, it generates random patterns of that particular size.

B. MISR (Multiple Input Signature Register)

A Multiple Input Signature-analysis Register (MISR) is one which can be used to reduce the amount of hardware required to compress a multiple bit stream. The MISR provides an alternative to using multiple Linear Feedback Shift Registers (LFSRs) in parallel and separately comparing the error polynomials.

Test patterns for BIST can be generated at-speed by an LFSR with only a clock input. Then the outputs of the DUT (Device under Test) must be compared to the known good response which is termed as the golden signature. In general, collecting each output response and offloading it from the DUT for

comparison is too inefficient to be practical. This will consume a huge storage capacity. A reasonable solution is to make some form of data compression on these responses before making the reference comparison. In order to compress the entire output stream into a single signature value, a multiple input signature analysis register can be used. The compressed response is referred to as the signature of the Device under Test. Signature analysis is the most popular compaction technique used today. Multiple-input signature register (MISR) is the solution that compact all outputs into a single LFSR. It works because LFSR is linear and obeys superposition principle.

All responses are superimposed into one LFSR. The final remainder is the XOR sum of remainders of polynomial divisions of each Primary Output by the characteristic polynomial. Its output develops a signature based on the effect of all the bits fed into it. If any bit is wrong, the signature will be different from the expected value and a fault will have been detected.

C. MISR Implementation

A parameter based Generalized MISR has been designed for this project. It is because in this programmable MIST when we give the size as input, it generates random patterns of that particular size.

The theory of its operation can be stated simply as follows. An m-bit input (one from each input line) is added, modulo 2, to the contents of the m D Flip-flops constituting the register). The result is shifted one position before the next word is added. After the last input bit is added, the remaining contents of the D Flip-flops are aggregated to give the output signature. The initial contents of the flip flops are assumed to be zeros and then the input values are fed in parallel.

D. BIST Controller

BIST controller is the most important part of the BIST system which coordinates the operations of different blocks of the BIST. Based on the test mode input to the controller, the system either operates in the normal mode or in the test mode. When the TM is 1, the system enters the test mode, it gives enable signal to the LFSR which generates the patterns which are fed as inputs to the DUT and then it gives enable signal to MISR for the compression of patterns from the DUT. It is the controller which decides for how many cycles the enable needs to be made 1 based on the length of the scan chains which is Shift Size and the input-output size of the DUT. The BIST controller that we designed follows the STUMPS Architecture and has a state machine that controls the BIST session. The states that were assumed in the state machine are: **RESET, GenData, Shift Data, Normal Mode, GenSignature, and Exit**. The controller actually applies the test. This consists of loading the scan chains with data, handling the scan

enable pin for data capture, shift enable for Shifting data into scan chain and then unloading the scan chains.

E. DUT (I2C Slave)

The system that is to be tested is termed as the Device under Test or the DUT. It is the circuit of the IC that is going to be checked for any defects after its manufacturing. The BIST scheme checks for any physical defects that are bound to occur in the IC namely bridging faults, and most importantly stuck-at faults. Any digital design represented in one of the Hardware Description Languages (HDL's) is used as a DUT. The BIST controller gives the input size to the LFSR and enables it. It generates random patterns of that size and is fed to the DUT. The DUT is converted into scan chains for the purpose of testing. When the inputs to the DUT is given, the scan chain works according to the shift-capture loop, generates some output which is then given to the MISR for compression. If the particular circuit is faulty, then the Patterns generated by the circuit in response to the LFSR Output will be different from the golden values of the circuit the first DUT that we have used is I2C Slave and I2C SlaveIP is taken from the Open core sites and Three Scan chain is inserted by using DFT Compiler (SYNOPTSYS EDA Tools).

F. Signature Analyzer

Signature is a term which refers to any statistical property which is capable of distinguishing between good and bad circuits. We do the signature analysis by comparing the signature obtained with the golden signature. Golden signature refers to the good machine signature which is the output of the MISR when the circuit is working perfectly. We compare the actual signature, which is the compressed output from the MISR, generated during the testing procedure with the golden signature, which has already been evaluated and stored. If any discrepancy is found we say that the circuit is faulty.

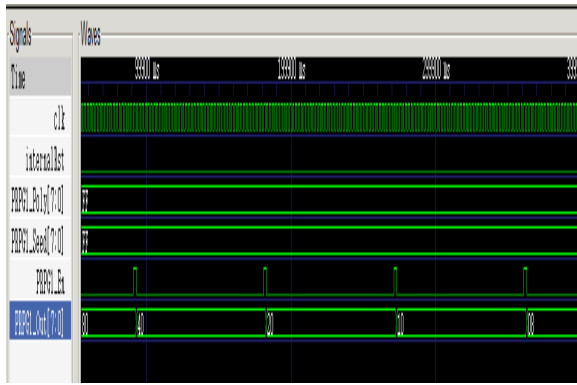
There are rare chances of error when aliasing occurs. Aliasing means the bad machine signature equals good Machine signature and hence produces erroneous output and it is resolve by using more bit Size MISR.

VII. Tools USED

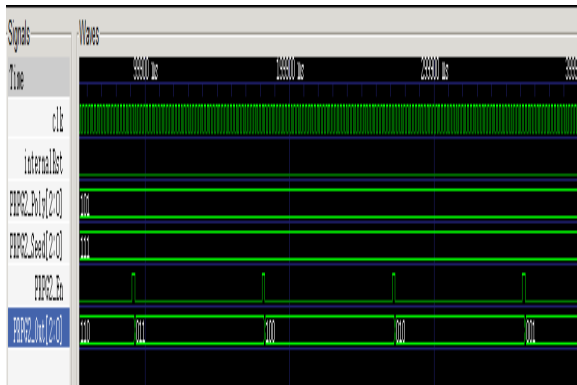
- VCS – Simulation(DVE GUI)
- Icarus VERILOG –RTL Design
- Design Compiler – Synthesis
- DFT compiler –Scan insertion
- GTKWave –Waveform Viewer

VIII. SIMULATION RESULTS(GTKWave)

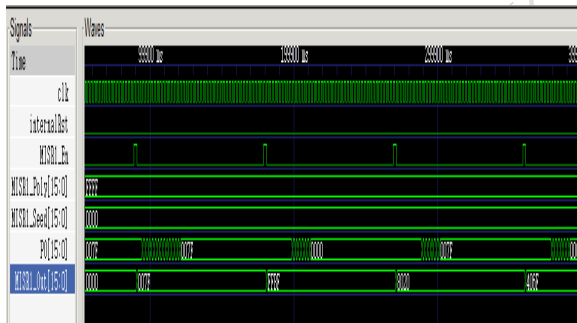
1. PRPG1 (Pseudo Random Pattern Generator)



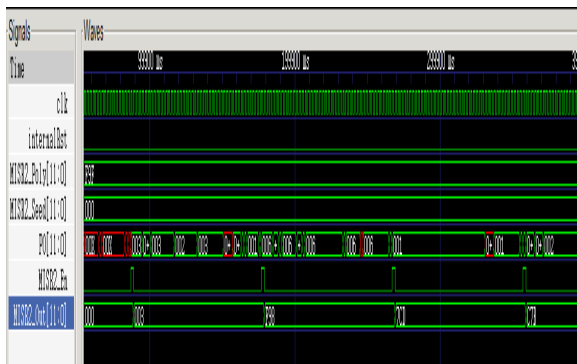
2. PRPG2 (Pseudo Random Pattern Generator)



3. MISR1 (Multiple Input Signature Register)



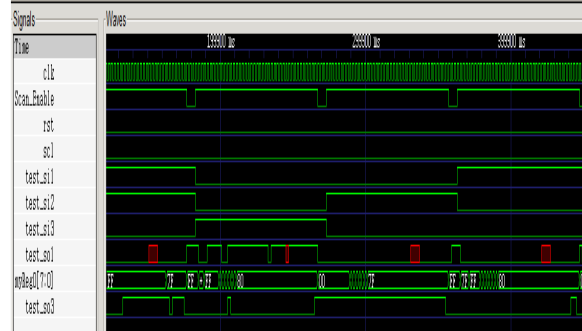
4. MISR2 (Multiple Input Signature Register)



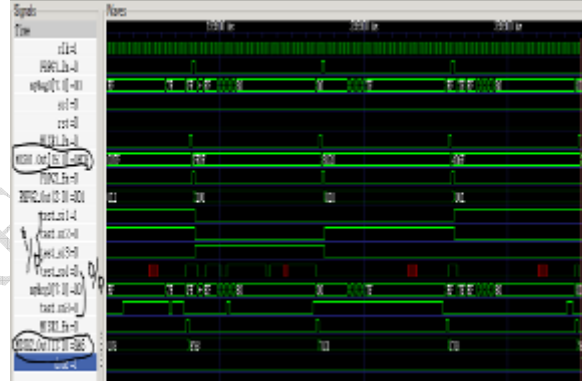
5. BIST Controller



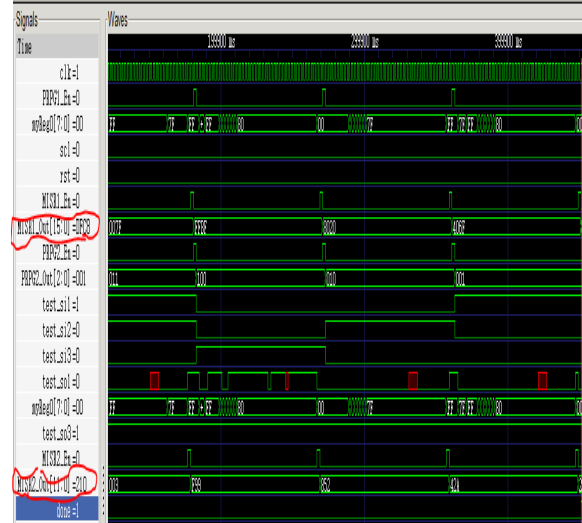
6. Integrated TOP Level BIST Module



7. Fault Free DUT (I2C Slave) Signature



8. Faulty DUT (I2C Slave) Signature



IX. CONCLUSION

The process of testing involves driving control signals from an inbuilt controller, generating pseudo-random patterns on the chip using LFSR, passing the patterns through the DUT, compact the responses

from the DUT into signatures, passing it through the signature analyzer for analyzing these signatures to match with the golden values and finally giving out the pass or fail signal.. For a particular IC, the size is fixed and hence with just the clock signal and the test mode signals the particular IC can be tested. The output is also simplified with just the single signal indicating the pass or fail status after the signature analysis. The Logic BIST is highly efficient with a high fault coverage of above 90-95% and can be seen when combined with a fault coverage estimation tool and the best part of the scheme is that it is at-speed which reduces the interface to the tester, tester memory and tester time.

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