DESIGN OF DDR SDRAM CONTROLLER FOR EMBEDDED SYSTEM

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***ABSTRACT*:** *DDR SDRAM (Double Data Rate Synchronously Dynamic RAM) is SDRAM with 2n prefetch architecture. DDR SDRAM most commonly used in various embedded application like signal processing, networking, image/video processing etc which need more and more cheap and fast memory. The memory controller accepts commands using local interface and translates them to the command sequences required by DDR SDRAM devices. How over there are challenges in its controller design those are arising to its straight requirement much as regular refresh operation, memory initialization process, proper active and precharge command etc. The principle and commands of DDR SDRAM controller design are explained in this paper. The operations of DDR SDRAM controller are realized through Verilog HDL .This proposed architecture design of DDR SDRAM controller is used as IP core into any FPGA based embedded system having requirement of high-speed operation.*

***Keywords—DDR SDRAM, DDR SDRAM controller, SDRAM*, Verilog, DRAM, FPGA, Embedded system**

1: INTRODUCTION

Single data rate (SDR) SDRAM that drives/latches data and command information on the rising edge of the synchronous clock. DDR SDRAM is a type of SDRAM that inherits technologies from SDR SDRAM and realizes faster operation and lower power consumption.DDR SDRAM achieves a data transfer rate that is twice the clock frequency by employing 2-n bit prefetch architecture [3].In this architecture, 2n bits of data are transferred from the memory cell array to the I/O buffer every clock. Data transferred to the I/O buffer is output n bits at a time every half clock (both rising and falling edges of the clock (CK)).

The proposed memory controller shown in figure 1 used to interface memory to other rest of the embedded system. Several task like refresh management, initialization, command generation, address mapping etc are done by memory controller. This Memory controller design has implemented in RTL in Verilog. The focus of this work is to implement design of DDR SDRAM controller which provide memory interface between the DDR SDRAM memory module and main embedded system. Top level model is shown in fig.1.The design contains the DDR SDRAM controller between the Host and the DDR SDRAM memory.

2: DDR SDRAM

A single read or write access for the DDR SDRAM effectively consists of a single 2*n*-bit wide, one clock- cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half clock-cycle data transfers at the I/O pins. As the internal bus width is twice the external bus width, DDR SDRAM achieves a data output rate that is twice the data rate of the internal bus.

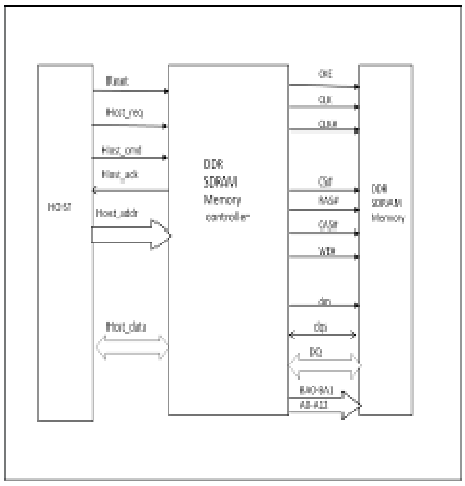

Fig.1 Top level Block Diagram of DDR SDRAM Controller for FPGA based embedded system

Double data rate (DDR) SDRAM—SDRAM that latches command information on the rising edge of the clock; data is driven/latched on both the rising

and falling edges of the clock rather than just the rising edge. This doubles data throughput rate without an increase in frequency.

DDR SDRAM employs a differential clock (CK, /CK) and data strobe signal (DQS) to realize high-speed data transfer. DQS is synchronized with CK, and data input/output (DQ) is synchronized with both the rising and falling A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver[5]. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

3. DESIGN OF DDR SDRAM MEMORY CONTROLLER

The functional block diagram of the DDR controller is shown in Fig.2. It consists of four modules, Control Interface, Address Mapping, Refresh management, Control FSM and Command generation, Data path.

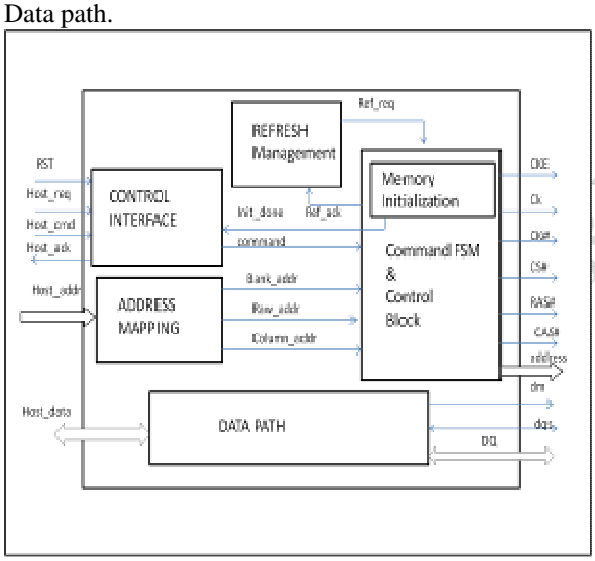

Fig 2 Architecture of DDR SDRAM Controller

Control Interface Module Control Interface Module accepts command from embedded system and decoding the command and providing the request to the Command module

Address generation module The DDR memory controller receives DDR memory access requests along with a 27-bit logical address from the rest of the system/Host.DDR2 memory controller uses the logical address to generate a

Row, column, and bank address for the DDR SDRAM. The generated bank address (BA0, BA1), ROW address, Column address is given to the control FSM and command generation module.

Command FSM and control generation

This module accepts command from the Control Interface Module and bank, row and column address from the address generation module and generating the proper commands to DDR SDRAM. This module handles read, write and refresh operation of the DDR SDRAM.

This module also takes care of initializing DDR SDRAM. Prior to normal operation, DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures, other than those specified, may result in undefined operation. Her core is taken to handle this procedure.

Refresh control Similar to the other DRAMs, memory refresh is required. DDR memory controller begins performing refreshes at a rate defined by the refresh rate bit in the SDRAM refresh control register

Data Path The data path module performs the data latching and dispatching of the data between the Processor and DDR Memory.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 4 locations. An auto precharge function may also be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

4. FUNCTIONAL DESCRIPTION & IMPLEMENTATION

a) Initializing Memory

Prior to normal operation, DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Apply stable clocks.DDR SDRAM requires a 200µs delay prior to applying an executable command [3]. Once the 200µs delay has been satisfied, a DESELECT or NOP command with CKE high should be applied. Following the NOP command, a PRECHARGE ALL command should be applied. Wait at least tRP time; during this time NOPs or DESELECT commands must be given. Next a LOAD MODE REGISTER command should be issued. Wait at least tMRD time; only NOPs or DESELECT commands are allowed [3].

A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state. Once in the idle state, two AUTO REFRESH cycles must be performed (tRFC must be satisfied.) Additionally, a LOAD MODE REGISTER command for the mode register is issued.

b) MODE Register Definition

The mode register is used to define the specific DDR SDRAM mode of operation. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode. The mode register is programmed via the LMR command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is reprogrammed again or until the device loses power (except for bit A8, which is self-clearing)[3].

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specifies the CAS latency, and A7-A12 specifies the operating mode [3]. Fig.3 shows the description of mode register [3].

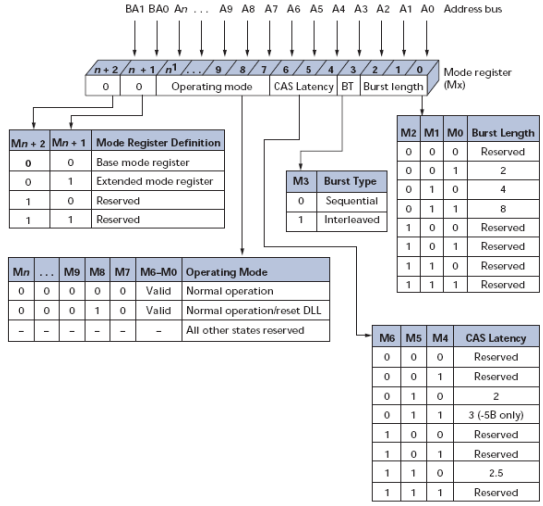

Fig.3 Memory Mode register

c) DDR SDRAM Memory commands

Table 1 presents the commands issued by the controller. These commands are passed to the memory using the following control signals [3]. The memory interface control signals and its timings are referred from Memory device Datasheet from Micron Technology [3].

- Row Address Select (RAS)
- Column Address Select (CAS)
- Write Enable (WE)
- Clock Enable (CKE)
- Chip Select (CS) (always held Low during device operation)

Function	CS	RAS	CAS	WE	Addr
DESELECT	H	X	X	X	X
NOP	L	H	H	H	X
ACTIVE	L	L	H	H	Bank/row
READ	L	H	L	H	Bank/col
WRITE	L	H	L	L	Bank/col
Burst Terminate	L	H	H	L	X
PRECHARGE	L	L	H	L	CODE
AUTOREFRESH	L	L	L	H	X
LOAD MODE REGISTER	L	L	L	L	OPCODE

Table 1 DDR SDRAM Memory commands

DESELECT

The DDR SDRAM is effectively deselected using this command. The DESELECT function (CS# HIGH) prevents new commands from being executed to the DDR SDRAM. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER (LMR)

The Mode register is used to define the specific mode of DDR SDRAM operation, including the selection of burst length, burst type, CAS latency, and operating mode. The mode registers are loaded via inputs A0–A*n*. The LMR command can only be issued when all banks are idle.

ACTIVE (ACT)

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access, like a read or a write The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*n* selects the row. After a row has been opened, READ or WRITE commands can be issued to that row. A PRECHARGE command is also issued by the controller to deactivate the open row. The controller also issues another ACTIVE command to the new row.

READ

The READ command is used to initiate a burst read access to an active row, the value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given density) selects the starting column location. After the read burst is over, the row is still available for subsequent access until it is precharged [5].

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given density) selects the starting column location [5].

PRECHARGE (PRE)

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The value on the BA0, BA1 inputs selects the bank, and the A10 input selects whether a single bank is precharged or whether all banks are precharged.

BURST TERMINATE (BST)

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled).

The most recently registered READ command prior to the BURST TERMINATE command will be truncated. The open row from which the READ burst was terminated remains open.

AUTO REFRESH (AR)

AUTO REFRESH is used during normal operation of the DDR SDRAM This command is non persistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued. The REFRESH command instructs the controller to perform an AUTO REFRESH command to the SDRAM. The controller will acknowledge the REFRESH command with a ACK.

c) Command FSM and Control generation

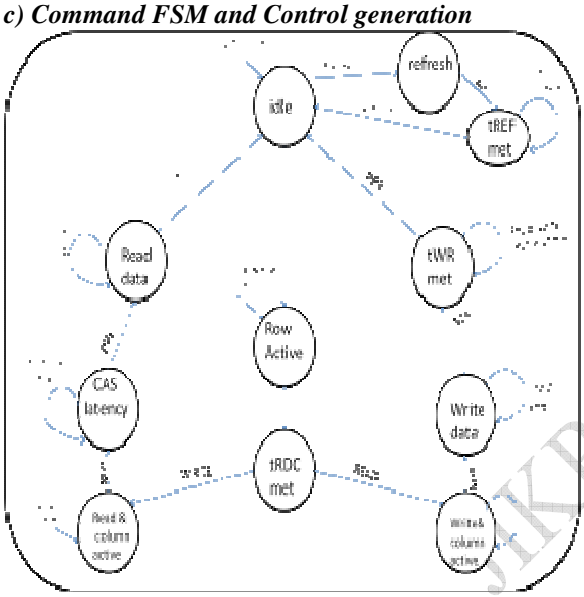

Fig. 4 state diagram of Command FSM and control module

The fig. 4 shows the state diagram of command generation and control FSM, which handles read, write and refresh of the DDR. The Command generation and control FSM state machine is initialized to idle during reset.

After reset, control FSM stays in idle as long as initialization done is low which indicates the DDR initialization sequence is not yet completed. From this state, a READ/WRITE/REFRESH cycle starts depending upon host_address, host_req, host_cmd, ref_req. All rows are in the "closed" status after the DDR initialization. The rows need to be "opened" before they can be accessed. However, only one row in the same bank can be opened at a time. Since there are four banks, there can be at most four rows opened at the same time. If a row in one bank is currently opened, it needs to be closed before another row in the same bank can be opened. ACTIVE command is used to open the rows and PRECHARGE is used to close the rows. When issuing the commands for opening or closing the rows, both row address and bank address need to be provided.

In this design, the ACTIVE command will be issued for each read or write access to open the row. After a tRCD delay is satisfied, READ or WRITE commands will be issued .Read or write is determined by the host_cmd status, according to host_cmd the state machine switches to write state for writing the Data to memory and the state machine switches to Read state for reading data from memory.

Read cycles, the state machine switches from, Read state to CAS latency state, and then switches to crate for transferring data from DDR to Host. The burst length determines the number of clocks the state machine stays in read data state. After the data is transferred, it switches back to idle and it will also acknowledge the host for completion of read operation. For write cycles, the state machine switches from Write state to write data state for transferring data from host to DDR, then switches to t WR met state After the clock rising edge of the last data in the burst sequence, no commands other than NOP can be issued to DDR before write recovery time (tWR) is satisfied. It will also acknowledge the host for completion of write operation.

Different states of Command FSM

1) Refresh state

DDR memory needs a periodic refresh to hold the data. Refresh request is generated by activating ref_req signal of the controller. The ref_ack signal will acknowledge the recognition of reg_req and will be active throughout the whole refresh cycle. Note that no system read/write access cycles are allowed when ref_ack is active. This periodic refresh is done using AUTO REFRESH command. All banks must be idle before an AUTOREFRESH command is issued. In this design all banks will be in idle state, as every read/write operation uses auto precharge.

2*) Active state:*

The ACTIVE command is used to open a row in a particular bank for a subsequent access, like a read or a write. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*n* selects the row.

3) Read state:

The READ command is used to initiate a burst read access to an active row, as shown in Fig.4. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given density and configuration) selects the starting column location.

4) *Write state:*

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where A*i* is the most significant column address bit for a given density and configuration) selects the starting column location.

d) Data Path Module

The data flow design between the SDRAM and the system interface. The module in this reference design interfaces between the DDR SDRAM with and the Host data bus.

The design handles burst length up to 4.The data path contains Read FIFO and Write FIFO. The data path module performs the data latching and is dispatching of the data between the processor and DDR.

5. TIMING DIAGRAMS

The fig.5 and Fig.6 are the read cycle and write cycle timing diagrams of the reference design with the two CAS latency cycles and the burst length of four. Following timing for read and writes cycle is as per memory manufacture datasheet. The controller matches all the timing requirement of the memory manufacture as per JEDEC standards [9].

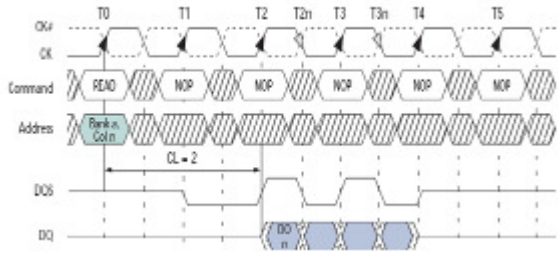

Fig.5 Read cycle timing diagram [3]

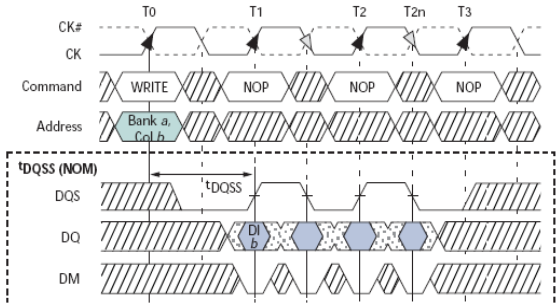

Fig. 6 Write cycle timing diagram [3]

6. SIMULATION RESULTS

The DDR controller design is developed by Verilog [4].**S**imulation results for refresh, Read and Write cycle is as following.Fig.7, fig.8, fig.9, fig.10 waveforms of shows refresh module, read operation and write operation.

a)Refresh operation

Refresh_count is loaded with refresh count value which is decremented every clock cycle. When refresh_count become 0000 the refresh_req is generated.

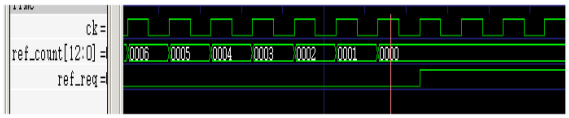

Fig. 7 Refresh counter

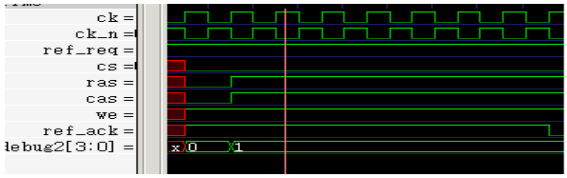

Fig.8 Auto refresh command generation

When ref_req set to high, the AUTOREFRESH command issued to memory for periodic refreshing. Auto refresh command period has to be matched for proper refreshing. On completing auto refresh the ref_ack set to low. Thus the refresh count value is again restored in the register.

b)Read operation

In the Read operation the data with DQS signal coming from the memory which is latched at data path module.

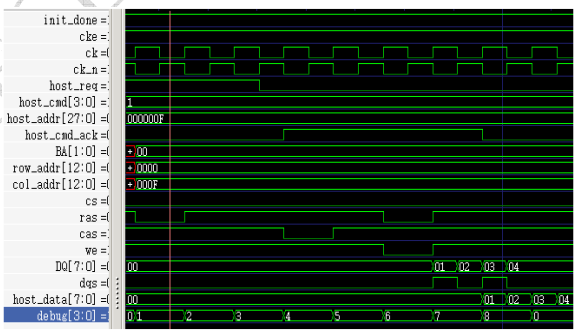

Fig. 9 Read operation

c)Write operation

In the Write operation the data with DQS signal and DM(data mask) signal coming from the memory controller to Memory.

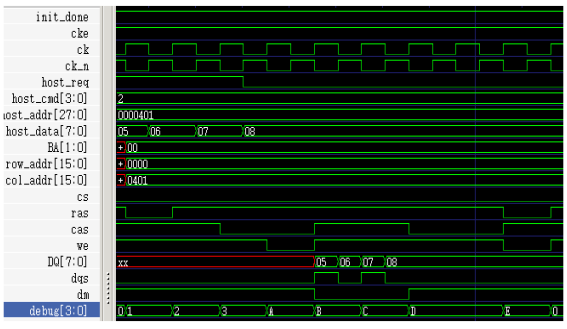

Fig. 10 Write operation

7. CONCLUSIONS

In this work propose architecture of a High speed DDR SDRAM Controller with burst data transfer which synchronizes the data transfer a between DDR SDRAM and rest of the Embedded system. The Micron DDR Memory model (JEDEC Standard) is taken for the reference. This memory controller can be used in FPGA base embedded system design. The advantages of this controller are synchronizes the data transfer and burst oriented data transfer. The core is developed by using Verilog HDL [4]. This Design is verified by using test bench and several test cases, which cover most of the functionality of the design. The simulations of specified functions were conducted by the Icarus Verilog and Altera Quartus II 9.0.

8.REFERENCES

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APPENDIXES

IP	Intellectual property
FPGA	Field-programmable gate array
ASIC	Application-specific integrated circuit
MB	Megabyte
RAM	Random Access Memory
DDR	Double Data Rate
SDR	Signal Data Rate
FIFO	First In First Out
FSM	Finite State Machine
CAS	Column Address Strobe
RAS	Row Address Strobe