

# Design and Implementation of 4-QAM Architecture for OFDM Communication System in VHDL using Xilinx

<sup>1</sup> Mr.Gaurang Rajan , <sup>2</sup> Prof. Kiran Trivedi <sup>3</sup> Prof.R.M.Soni

<sup>1</sup>PG student (EC), S.S.E.C., Bhavnagar-Gujarat  
rajantrust@gmail.com

<sup>2</sup>Associate professor, Electronics and Communication Department,  
S.S.E.C., Bhavnagar-Gujarat  
ktrivedi@gmail.com

<sup>3</sup>Assistant professor, Electronics and Communication Department, LCIT, Bhandu-Gujarat  
rajnikant.soni@lcit.org

**Abstract:** Data on OFDM subcarriers is mapped (modulated) using common digital modulation schemes IEEE 802.11a/g WLANs uses BPSK, QPSK, 16-QAM, 64-QAM. Choice of QAM is to provide both phase and amplitude vary so we can use more number of sub channels in band. Also contain higher data rate then QPSK. Implementation of QAM is satisfies the specifications of the IEEE 802.11a/g. this architecture of QAM leads to power and area saving.

**Index Terms:** QAM, OFDM, ASK, PSK

## 1. INTRODUCTION

Among all the forms of digital modulation used in communication system a more interesting is QAM (Quadrature Amplitude Modulation). In this system (as said), the digital signal to be transmitted is acts both on amplitude and as on the phase of the carrier signal. Therefore, QAM modulation is a mix of ASK with PSK.

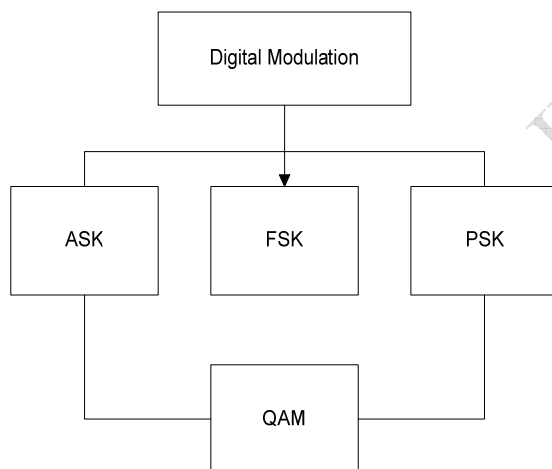


Fig1. Construction of QAM

Because of the orthogonality of the carriers it can use the same frequency band, where each carrier may be adjusted independently and transmitted through the same frequency. Figure 1 shows design of QAM. It contain mixed of both modulation scheme like Amplitude shift keying(ASK) and phase shift keying(PSK).

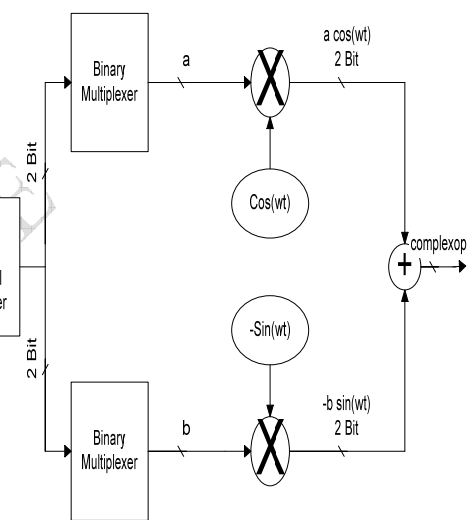


Fig2. Diagram the QAM modulator

## 2. DESIGN OF QAM

To make it possible two carriers with the same frequency and phase in 90 degrees (sine and cosine) are modulated in amplitude by a multilevel signal (Figure 2), which through a multilevel binary converter generates the levels often a and b according to the number of binary input. For example, on a QAM modulator of two bits a one bit is sent to the converter in phase and the other bit is sent to the converter in quadrature. Now for a modulator of four bits two bits are sent to the converter in phase and the other two are sent to the converter in quadrature.

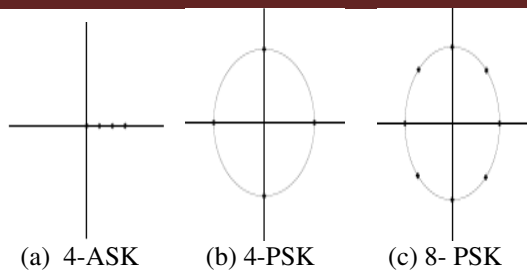


Fig3. Diagrams constellation of ASK and PSK

**2. A MODULATION**

The result of the sum of these signals is a signal modulated both in phase and in quadrature

$$S(t) = a \cos(\omega t) - b \sin(\omega t)$$

$$= \sqrt{a^2 + b^2} \cos\left(\omega t - \arctan\left(\frac{b}{a}\right)\right) \dots\dots\dots 1$$

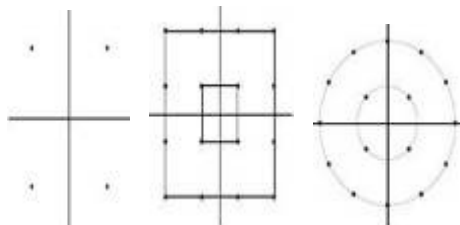
The equation (4.1) represents the signal with a certain amount of amplitude and phase and phase is possible to use a representation of that signal:

$$S(t) = \sqrt{a^2 + b^2} \angle -\left(\arctan\left(\frac{b}{a}\right)\right) \dots\dots\dots 2$$

$$S(t) = a + jb \dots\dots\dots 3$$

As a and b there are some discrete levels, then we can give a diagram all possible combinations of a and b, called Diagram of constellation Figure 3 shows the diagram, constellation for modulation ASK and PSK.

The architecture diagram of a QAM modulator is mounted according to the discrete levels produced by the converter. Thus in a QAM modulator of two bits have only four points in the constellation, so this modulator is called as 4 QAM (Figure 4 (a)). Similarly in QAM modulator is of 4 bits and 16 QAM are so on. Note that there are several ways to implement the QAM constellation (Figure 4 (b) and Figure 4 (c)). The format of the constellation is determined by the conversion of angle.



(a) 4-QAM (b) 16-QAM (c) 16-QAM

Fig4. Constellation representation of QAM

**2. B ENCODER'S CONSTELLATION**

The constellation maps of the encoder of the channel of Mn bits are at a point  $A_n + jB_n$  in the constellation diagram of the modulator. The decoder receives this point as how Mn Bits are transmitted. As said, it is important to note that this mapping made just one conversion from bits to the phase as represents, but it made no modulation. And need

Specify how the constellation will be mapped, in order to implement this block However, regardless of the format of the constellation the block of the encoder can be done through a query to a table of conversion and implemented by the LUT that is in the ICs of FPGAs.

For example, a 4-QAM constellation, shown in Figure 4(a), so that a and b are Binary numbers of 3 bits in addition two and have a value of 010b for the bit 0 or 110b for the bit 1 has the potential shown in Table 1.

BITS	Point
00	010 + j010
01	010 + j110
10	110 + j010
11	110 + j110

Table 1 Conversion table of 4-QAM

The input of encoding a number of binary bits Mn, is that the output generates two binary numbers one on phase and another on quadrature and whose size is defined by IFFT.

**2. C DECODER'S CONSTELLATION**

At receiver, the point of the transmitted constellation (Figure 4 (a)) may have changed (Figure 4.6) due to the sounds of the channel of transmission at the time of sampling error of receiver and several other causes.

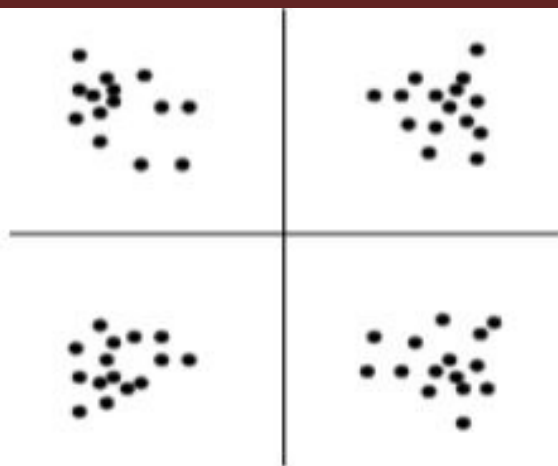


Fig5. Constellation in the receiver

The serial-parallel converter of the transmitter has the function to receive data to be transmitted, assembles them in blocks of M bits, and then separates them into N channels, with Mn Bits each. Remember that the number of bits in each channel may be different.

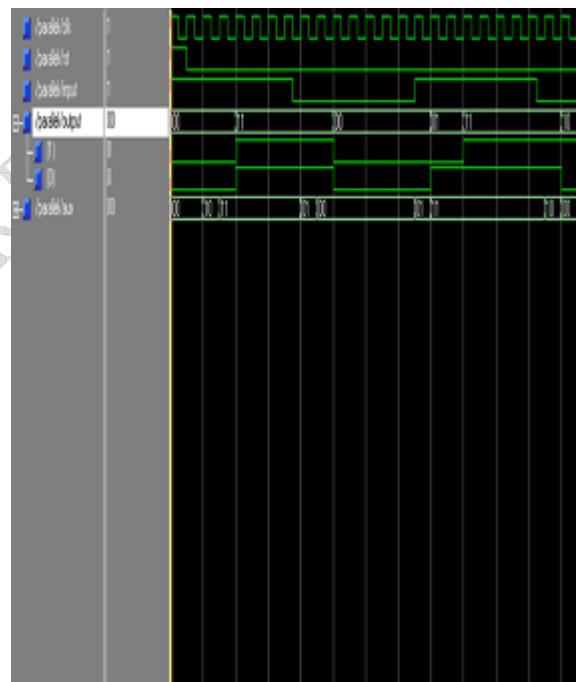


Fig6. Simulation result of s/p convertor

So that a decision can be made about what point in the constellation representing the signal received this. That is function of the decoder.

For system explained above, in the Table 1 the bit 0 is converted to 010 and bit 1 is converted to 110. In this case, the decoder is implemented in a simple, takes up the most significant bit (which indicates the signal) to do the decoding and regenerating a number of binary bits m.

For systems where the constellation diagram is greater or even the 4-PSK, shown in Figure 4. (b) Will be necessary to implementation of more advanced methods.

### 3. IMPLEMENTATION DETAIL AND RESULTS

As an important part of the OFDM, modulation of signal is necessary requirement. So QAM is the modulation as well as demodulation techniques for the model. Apart from it there are other modulation techniques is also used like QPSK.

Here we write the QAM code on VHDL using Xilinx ISE 9.2i and Simulation result observe in Modelsim SE6.2c. Further results will be implemented it on the FPGA family Spartan Kit.

#### Serial to parallel

#### Multiplexer

In the multiplexer here we use two input of 12 bits

(real-a and real b and ima a and ima b) and one select line. When select line is zero or low at that time we get real a and real b as output, when select line is one or high we get ima a and ima b as output.

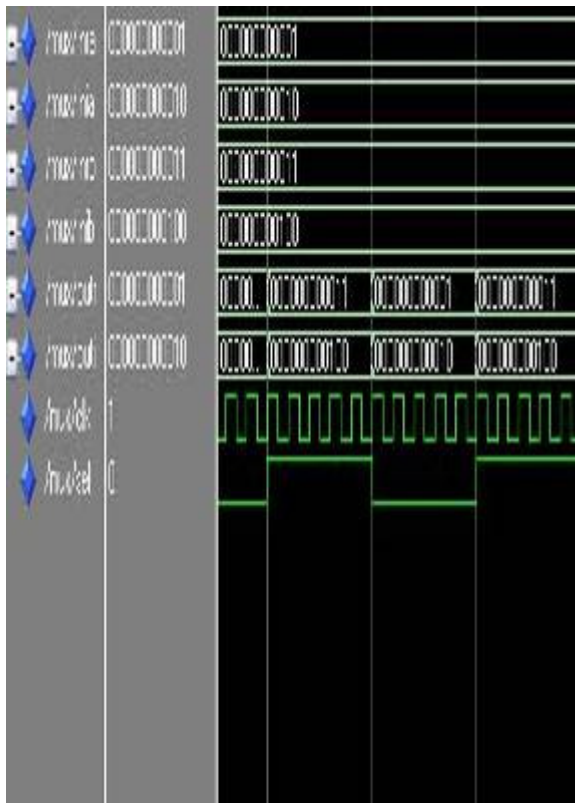


Fig7. Simulation result of Multiplexer

**QAM (Quadrature Amplitude modulation)**

In Quadrature Amplitude modulation techniques here we use two bit input as serially and it will be transmitted to the same bit multiplexer so it will generate the 4 point and 12 bit quadrature output with Different in phase and same in amplitude.

Here 12 bit stream to be indicate with:

- 0011.00000000= +1
- 1101.00000000= -1

As shown in result here we chose 2 bit stream for input so when reset line select as low or 0 then it will give the 4 point output in each quadrat with same amplitude and different phase. And when reset line select as high or 1 then it will give to 12 zero bit output.

In figure 8. Shows the RTL schematic of QAM and it gives the detailed of the various block and terminals of gate and flip-flops which is used to make LUTs and CLB, with Maximum Frequency: 134.012MHz.

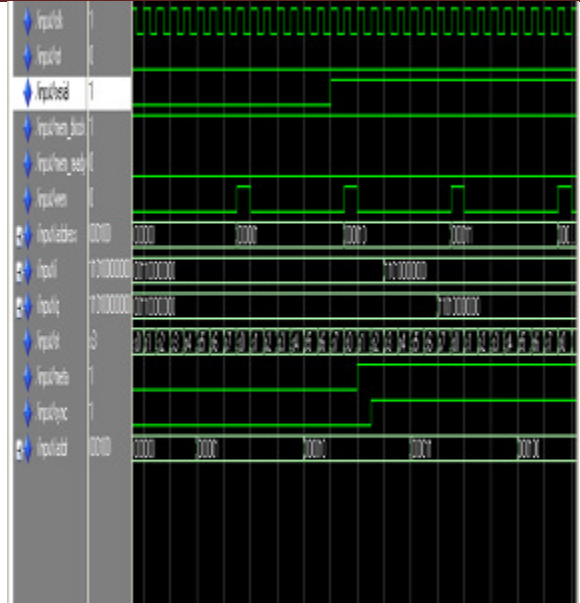


Fig8. Simulation result of QAM

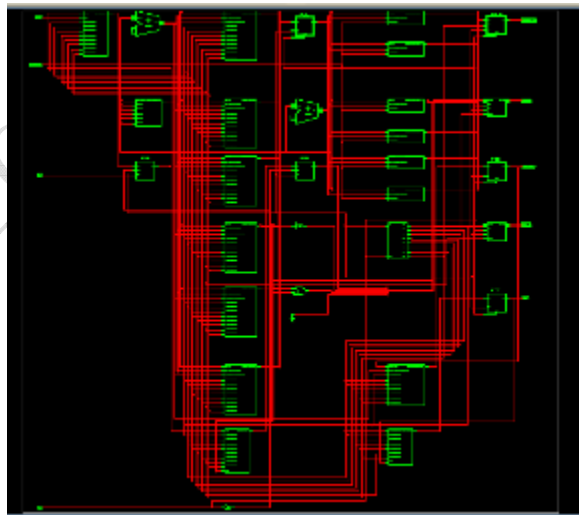


Fig9. RTL schematic of QAM

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	15	1,536	1%	
Number of 4 input LUTs	30	1,536	1%	
<b>Logic Distribution</b>				
Number of occupied Slices	19	768	2%	
Number of Slices containing only related logic	19	19	100%	
Number of Slices containing unrelated logic	0	19	0%	
<b>Total Number of 4 input LUTs</b>	<b>30</b>	<b>1,536</b>	<b>1%</b>	
Number of bonded IOBs	35	96	35%	
IOB Flip Flops	8			
Number of GLKs	1	4	25%	
Number of BCLKIOBs	1	4	25%	
<b>Total equivalent gate count for design</b>	<b>570</b>			
Additional 1745 gate count for IOBs	1,728			

Table 2 Design summary of 4-QAM

#### 4. CONCLUSION

4-QAM architecture is the most appropriate modulation scheme for OFDM based wireless broadband communication system because it contains higher data rate with less bandwidth and modeled with FFT/IFFT architecture instead of bank of modulation. It also satisfies the specification of IEEE 802.11 a/g is described in this paper. And implementation of this architecture is advantages of technology mapping in terms of time area and power consumption.

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