DESIGN AND ANALYSIS OF 256 BIT SRAM IN DEEP SUBMICRON CMOS TECHNOLOGIES

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ABSTRACT: *Todays' electronics world seek towards more and more low power and high speed performance. So, SRAM is embedding in every integrated circuit(IC) for better performance. This paper explores the design of 256 bit Static Random Access Memory (SRAM) with help of 6-T cell in 65nm and 45nm CMOS technology node, focusing on optimizing delay and average power dissipation, and also compared in terms of write access time, read access time and average power dissipation using LT spice IV and layout of 1bit memory has been performed using Microwind 3.1.*

KEYWORDS: 6-T SRAM cell, 65-45nm, layout, write access time, read access time, power dissipation.

1. INTRODUCTION

From the twentieth century to up to today, semiconductor electronics becomes more and more dominate in every area. Nowadays, it has become a global industry worth billions of dollars. Contemporary society uses all manner of electronic devices built in automated or semi-automated factories operated by the industry. Our daily lives are significantly affected by electronics, microelectronic technology. This is true on the domestic scene, in our daily life. Indeed, there is no doubt that revolutionary changes have taken place in a relatively short time and it is also certain that even more dramatic advances will be made in the next decades. This kind of domination of electronics industry has been arisen because of rapid advancement and drastically improvement in integration technology. Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a path toward both denser and faster integration. The transistors manufactured today are 20 times faster and occupy less than 1% of the area of those built 20 years ago. As the channel length is reduced, the performance improves, the power per switching event decreases, and the density improves. Domination of digital VLSI designs, on chip memory is more essential. Mostly, SRAM is used as a cache memory in modern SoCs and it is used SRAM memory is used in a lot of devices where speed is more crucial than capacity. Here SRAM implemented through deep submicron CMOS technology because of its low static power consumption fast switching and its noise immunity.

2. GENERALIZED SRAM ARCHITECTURE

Conceptually, SRAM architecture is drawn below. It consists memory cell array, write driver and pre-charge circuit, raw and column decoder, sense amplifier, data lines-data in and out. If numbers of

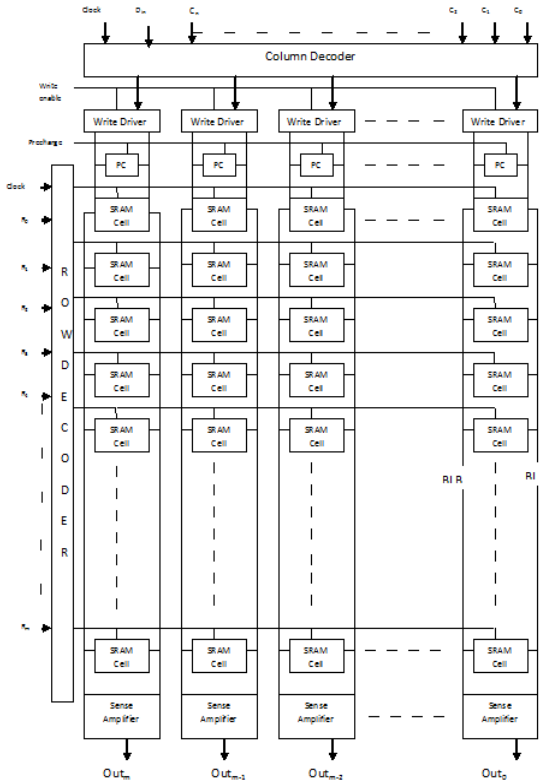

Fig.1 Detailed SRAM Architecture

address lines are m and numbers of data lines are n, then total size of memory can be obtained as 2^{m+n} where popular numbers of m and n are 8, 16, 32, 64, 256 etc. In this architecture, rows denote word lines which indicate for selecting particular memory cell and column denote bit and bit-bar lines for inserting and retrieving data from it. Separate write driver and sense amplifier are dedicated to each column for fast read and write operation. This architecture possesses fast write and read operation due to its differential writing and sensing scheme.

Memory cell

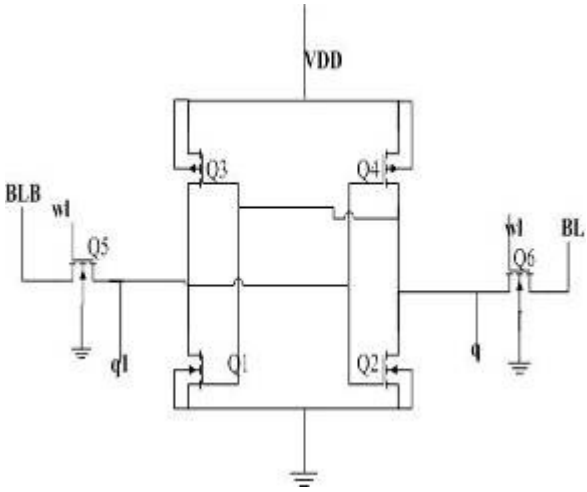

Fig.2 6-transistor memory cell

Memory cell is an essential element of SRAM which stores binary digit voltage level. A 6T CMOS SRAM cell is the most popular SRAM cell due to its superior robustness, low power and low-voltage operation. SRAM uses bistable latching circuitry to store each bit. The six-transistor (6T) SRAM cell is shown in fig. 2, in which Q3 and Q4 PMOS are pull up transistors, Q1 and Q2 NMOS are driver transistors. Access to the cell is enabled by the word line which controls the two access transistors Q5 and Q6 (NMOS as a pass transistor) which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins. The symmetric structure of SRAM memory cells also allows for differential signalling, which makes small voltage swings more easily detectable. This kind of memory cell retains state either 0 or 1 as long as power turn on which doesn't refresh periodically as DRAM cell.

Row and Column decoder

Address decoder is used to decode the given input address and to enable a particular Word Line (WL). In this SRAM design, two dynamic NAND CMOS decoder is used. One as a row decoder selects particular word line by raising up its voltage level and second as a column decoder selects particular column. For an n-word memory, an m: n dynamic NAND CMOS decoder is used where $n=2^m$. The schematic of 2:4 dynamic NAND CMOS decoder is shown in fig. 3.

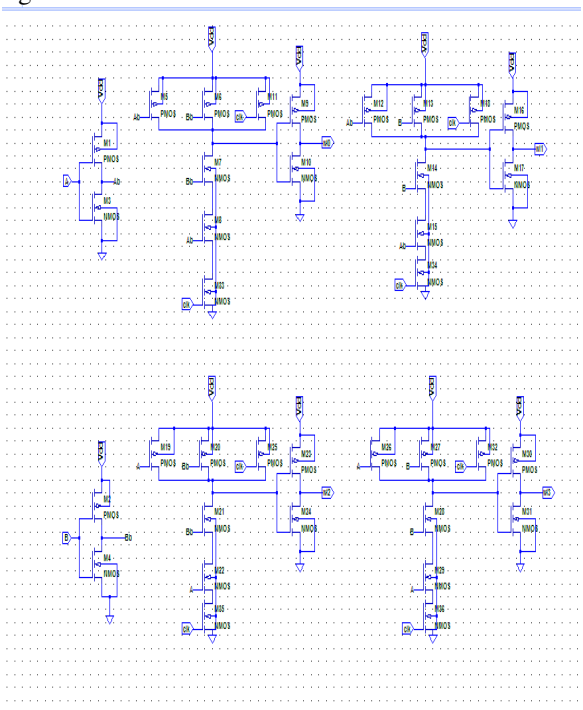

Fig.3 Decoder with Dynamic NAND Gate

Write driver circuit

The function of the SRAM write driver is to quickly discharge one of the bit lines from the pre-charge level to below the write margin of the SRAM cell. Normally, the write driver is enabled by the Write Enable (WE) signal and drives the bit line using full-swing discharge from the pre-charge level to ground. As shown in fig.4. Even though a greater discharge of the highly capacitive bit lines is required for a write operation, a write operation can be carried out faster than a read operation only one write driver is needed for each SRAM column. Thus, the area impact of a larger write driver is not multiplied by the number of cells in the column and hence the write driver can be sized up if necessary. Here, we are used basic CMOS inverter and NMOS pass transistors that form our write driver circuit.

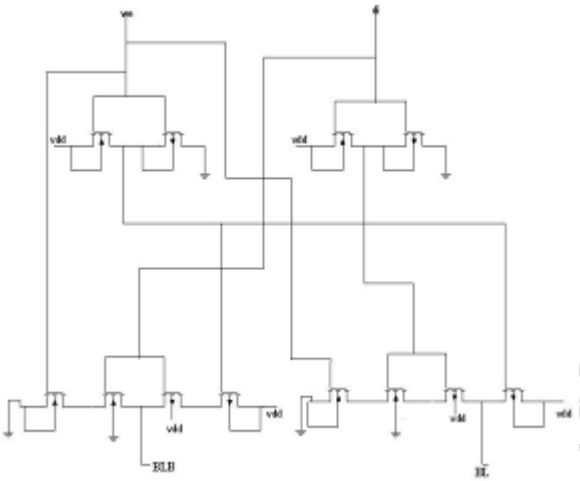

Fig.4 Write driver circuit

Pre-charge Circuit

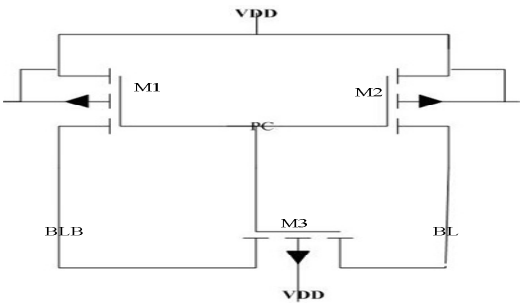

Fig.5 Pre-charge circuit

Pre-charge is used for pre-charging and equalizing of bit and bit-bar lines during data hold operation. For a better read and write operation. Here M1 and M2 PMOS are used for pre-charging and middle one for equalization. Generally, pre-charge voltage level is kept at $V_{DD.}$

Sense amplifier

Sense amplifiers are an important part in memory design. The read operation is typically the slowest memory operation, and as such defines the minimum delay of the SRAM cell. Bit lines experience a large capacitance due to their physical metal length and large number of cell access transistors connected to them. As a result, significant amount of time is required for a bit line to fully discharge. Rather than waiting for this to occur on its own, a sense amplifier is used to detect a small differential voltage on the bit lines, and quickly generate a full-swing output. The timing control of the sense amplifier and selection of load capacitors are critical for the correct functionality of the SRAM. If the Sense Amplifier Enable signal (SAE) is enabled before a sufficient amount of differential voltage is generated, the output may resolve incorrectly. If the sense amplifier is turned on too late however, the read time will be longer than necessary and excessive power will be dissipated. In latch-type sense amplifier, two cross coupled inverter is used with two capacitor connected at the ends. Capacitors store level of bit lines. After sensing levels of bit lines, positive feedback in the latch generates. That leads to a full amplification of the input signal to a full digital level.

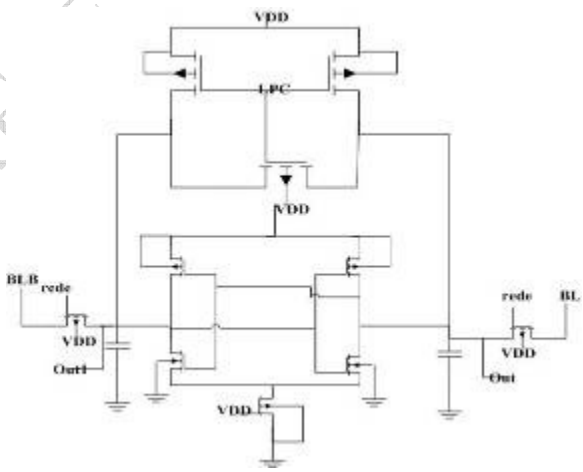

Fig.6 Sense amplifier with local pre-charge

3. SRAM OPERATION

Basically, SRAM operations are synchronized with its peripherals and given as data write, read and hold.

Write operation

The write operation means whatever data write into the SRAM cell. The write operation is similar to a reset operation of an SR latch. After one of the bit lines, BL in fig. 2, is driven from pre-charged value (V_{DD}) to the ground potential by a write driver through transistor Q6. If transistors Q4 and Q6 are properly sized, then the cell is flipped and its data is effectively overwritten. For a standard 6T SRAM Cell, writing is done by lowering one of the bit lines to

ground while asserting the word line at this time. Normally, to minimize the cell area and hence, increase the packing density, the sizes of the pull-up and access transistors are chosen to be minimal and approximately the same. However, stronger access transistors and/or weaker pull-up transistors may be needed to ensure a robust write operation under the worst process conditions e.g., in the fast PMOS and slow NMOS process skew corner.

Read operation

A Read operation means whatever data store in SRAM Cell, which is read by the sense amplifier. After applying read enable at access transistor of sense amplifier, same input at local pre-charge, and insertion of word line to memory cell, whatever data in memory cell appears at sense amplifier output node. For this operation status of memory has been explained. In read operation, the bit lines are pre-charged to V_{DD}. When these pre-charged lines connect with memory cell to sense amplifier, sense amplifier detects small difference of bit and bit-bar lines voltages and amplifies it through positive feedback. Here, 6T SRAM Cell has a differential read operation. This means that both the stored value and its inverse are used in evaluation to determine the stored value. The read operation is initiated by enabling the word line (WL) and connecting the pre-charged bit lines, BL and BLB, Sizing of Q1 and Q5 should ensure that inverter Q2–Q4 does not switch causing a destructive read. .A preferred sizing solution can be to use a minimum-width access transistors with a slightly larger than the minimal length channel and a larger than minimal width with a minimal length driver transistors.

Data hold operation

If the word line is not asserted, the access transistors will be isolated the cell from the bit lines. The two cross coupled inverters formed the two inverter connected back to back reinforce each other as long as they are disconnected from the outside world. And they will retain the data which they have already stored in the memory cell. In this state, pre-charge is activated.

4. SIMULATION WAVEFORMS

In this paper, schematic level file implemented on LT spice with PTM high performance CMOS model for 45nm and customized PTM CMOS model. And layout of 1 bit memory in 45nm has performed on Microwind.

As shown in fig. 7, write and read operation of 256 bit SRAM is described, where “clk” stands clock which is used for synchronization, “wl” stands for word line, “'di” stands for data input, “we” stands for write enable, “pc” stands for pre-charge, “q” denotes internal storage node of 6-T memory cell, and “q1” is invert node of “q”. “lpc” denotes active low local pre-charge for sense amplifier, “rede” denotes active low read enable, “out1” denotes output of sense amplifier and its invert at “ob1”. This waveforms depict whatever data appears at selected data line goes into enabled memory cell. After activation of sense amplifier and its local pre-charge, enabled memory cell has been read.

For 65nm technology, V_{DD}: 1.2V

For 45nm technology, V_{DD}: 0.9V

Technology node	Write access Time	Read access time	Average power dissipation
65nm	176.6ps	1.77ns	731.13µW
45nm	157.6ps	1.63ns	195.81µW

Table1 Comparison between 65nm and 45nm technology in terms of different parameters.

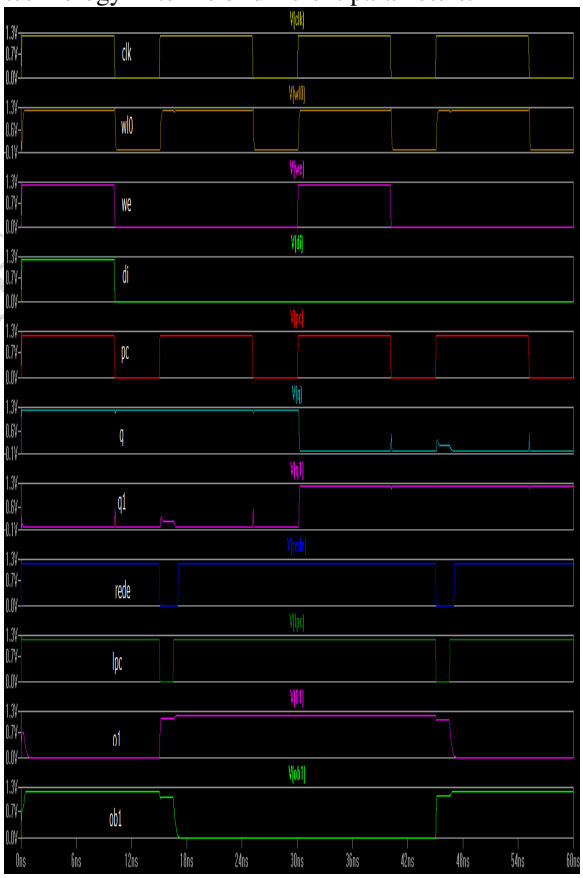

Fig.7 Waveforms of read and write operation of 256 (16*16) bit SRAM in 65nm CMOS technology

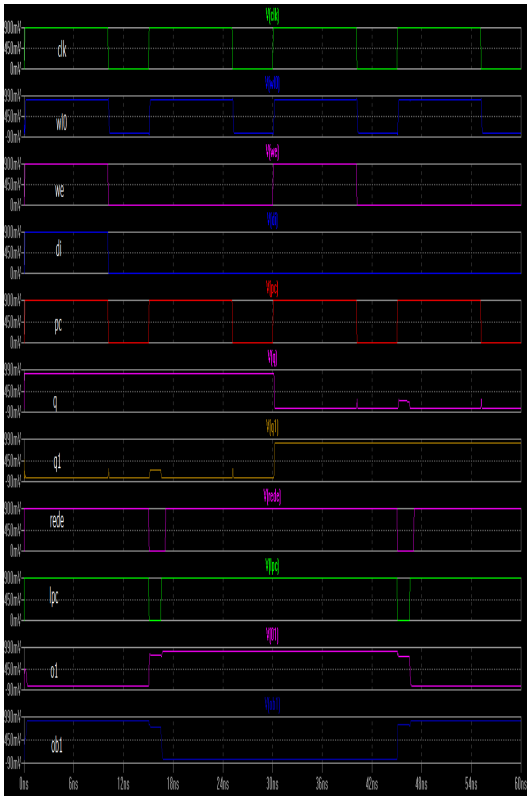

Fig.8 Waveforms of read and write operation of 256 (16*16) bit SRAM in 45nm CMOS technology

5. LAYOUT

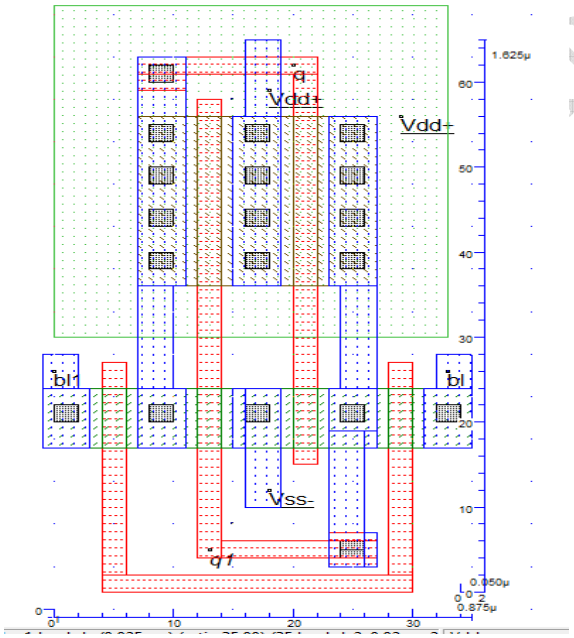

Fig.9 Layout of 6-T memory cell in 45nm technology

Here layout of 6-T memory cell is performed with cmos_45nm rule file and advanced BSIM4 MOS model on Microwind. This layout occupies 0.9675 μm^2 die area, and it is less than to the layout reported by "Low Voltage, Low Power SRAM Design" M.Tech (VLSI) project report.

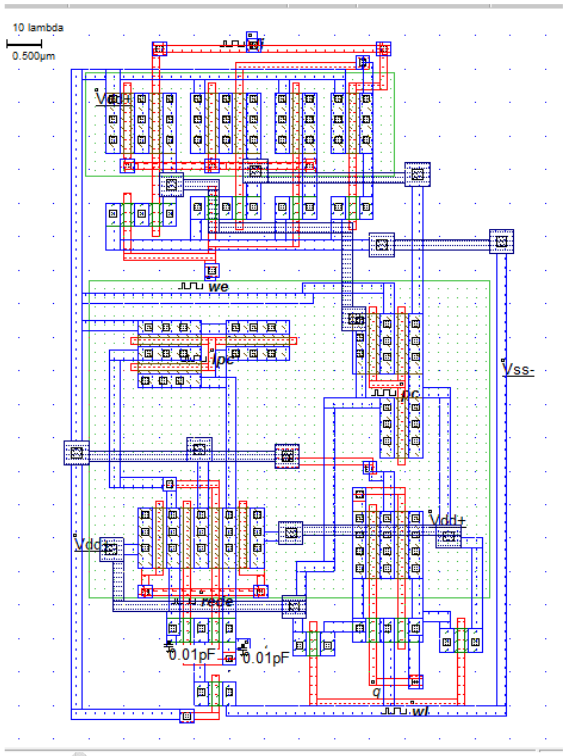

Fig.10 Layout of 6-T memory cell with its write and read circuitry in 45nm technology.

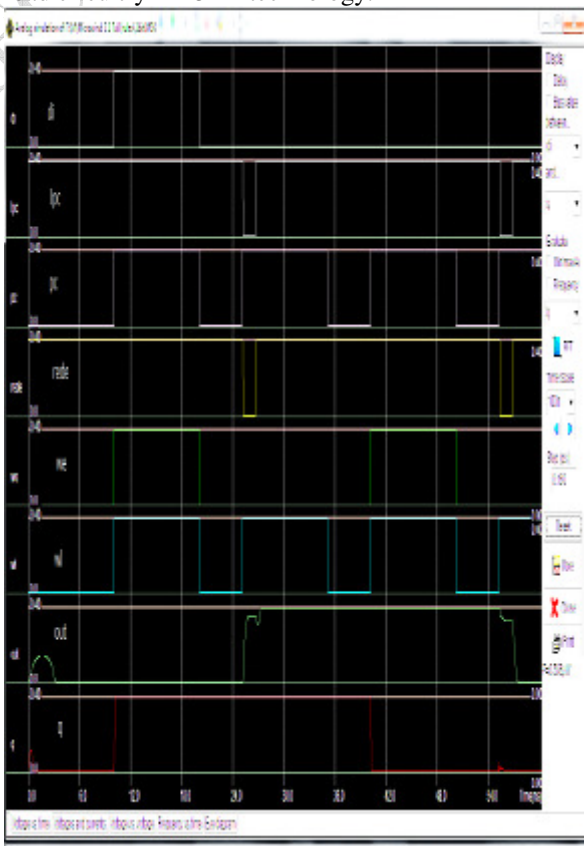

Fig.11 Analog simulation Layout of 6-T memory cell with its write and read circuitry in 45nm technology

In fig.10, layout of 6-T SRAM cell with its write and read Occupies die area 15.5775 μm^2 and it gives very less power consumption compared to its schematic level implementation and valued 0.508 µW.

6. CONCLUSION

From the results in smaller deep submicron technology node, we can conclude 256bit SRAM average power dissipation is 51.74%, average read access time is 5.105%, and average write access time is 18.555%, reduced in 45nm technology compared with 65nm technology respectively. Also in 45nm less area is required compared with 65nm. Subsequently, high performance and low power SRAM of different sizes is implemented .From the paper we also can conclude that average power is reduced in layout with respect to schematic.

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