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ASYNCHRONOUS RAM ADDRESS TRANSITION DETECTION CIRCUIT

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ABSTRACT — *In an Asynchronous semiconductor memory device, the change of address is immediately responded. So it also responds to such wrong address information and internal circuit selects the wrong address information and operates corresponds to that wrong address. The ATD circuit is used to avoid such problem. When any address signal changes it generates the pulse. And during that period an internal circuit of the memory device is held in the non-operating condition in response to change in address signal. And thus responding to wrong address information which is generated due to noise or deviation of timing in address signal is prevented by using ATD circuit.*

Key words:- **OFDM, STBC, SWTICHING, PATH FADING.**

1. INTRODUCTION

Pervasive computing demands that applications are capable of operation in highly dynamic environment without explicit user intervention Thus, pervasive applications are typically context-aware, to minimize user intervention To achieve context-awareness, pervasive applications need to be aware of whether contexts bear specified properties, thus being able to adapt their behavior accordingly. For example in an elderly care scenario, the application may specify a property *C*1: *the elder has been having meals, and then he tries to take medicine*, and send the elder an alarm that the medicine should be taken before meals, when the property *C*1 holds Among various contextual properties the application may specify, *dynamic properties*, which delineate the temporal evolution of the environment state, are of great importance. This is mainly due to the intrinsic dynamism of the pervasive computing environment. To cope with this dynamism, the context-aware application needs to keep a stretch of environment state evolution in sight, and use dynamic properties to delineate its concerns about the evolution. In the example above, the application is not concerned about specific status of the elder (e.g., "have meal" or "take medicine"). Rather, it is concerned with the temporal evolution of the elder's status that he was first having meals, and tries to take medicine right after the meal.

However, the specification and detection of dynamic properties is challenging, mainly due to that the computing entities in the pervasive computing environment coordinate in an asynchronous way and that the detection of contextual properties should be effectively conducted at runtime specifically, context collecting devices may not have global clocks and may run at different speeds. They heavily rely on wireless communications, which suffer from finite but arbitrary

delay. Moreover, context collecting devices (usually battery-powered sensors) may postpone the dissemination of context data due to resource constraints, which also results in asynchrony.

2. ASYNCHRONOUS RAM AND ADDRESS TRANSITION DETECTOR

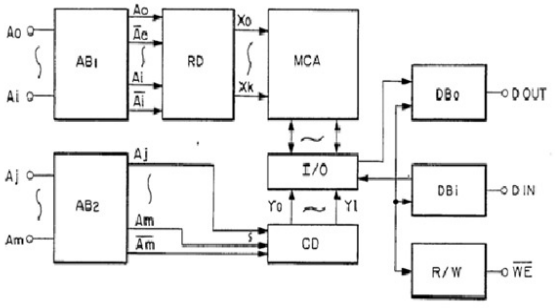

Figure 2.1: Block Diagram of the Conventional Asynchronous Semiconductor Memory Device

In this figure, AB_1, AB_2 are address buffers; RD is a row decoder; CD is a column decoder; MCA is memory cell array; I/O is an I/O gate; DBO is a data output buffer; DBi is a data input buffer R/W is a read/write controller; A0-Ai are row address signals; Aj-Am are column address signals; X0-Xk are row selection signals; Y_0-Y_1 are column selection signals; Dout is an output data; Din is an input data; WE is a write enable signal. The input address lines are applied to the address buffers AB_1 and AB_2. The

output of address buffers which are inverted and non inverted address lines is applied to the row and column decoder. Now according to the status of address lines the respected row (word line) and column (bit line) is selected in the memory cell array (MCA). On the other side depending on the status of the WE signal writing or reading operation is performed. For the writing operation the data Din to be written to the memory cell is passes through the input data buffer (DBi) to the I/O circuitry to the particular cell of the MCA. And for the reading operation the data stored in the memory cell is passes through the I/O circuitry to the output data buffer (DBo) to Dout.

3. ATD CIRCUIT

To avoid above said problem, the change in address signal is detected and hold the internal circuit to a non-operative condition in response to any change of address signal for a specified period. And this is accomplished by the extra circuitry which is called ATD (Address Transition Detection) circuit which generates the pulse of a specified period when one of the address signal changes. This circuit relates to an asynchronous semiconductor memory device and more specifically to a semiconductor memory device which has reduced power consumption as a result of holding an internal circuit to a non-operative condition in response to any change of address signal for a specified period following the change of said address signal

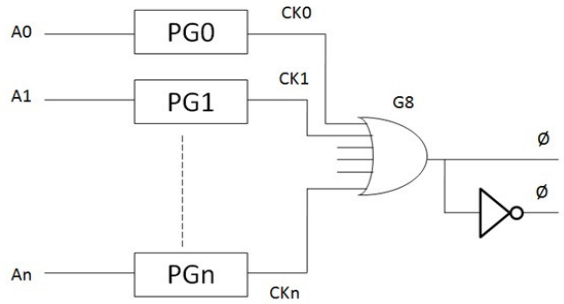

Figure 3.1: ATD Circuit

DESIGN OF SRAM

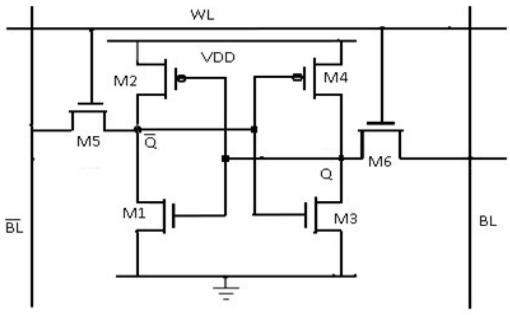

Figure 3.1.1: 6-Transistor CMOS SRAM Cell

The SRAM cell should be sized as small as possible to achieve high memory densities. To understand the operation of the memory cell, let us consider the read and write operations in sequence. Assume that a 1 is stored at Q. Further assume that both bit lines are precharged to 2.5 V before the read operation is initiated. The read cycle is started by asserting the word line, enabling both pass transistors M5 and M6 after the initial word-line delay. During a correct read operation, the values stored in Q and Q! are transferred to the bit lines by leaving BL at its precharge value and by discharging BL! through M1-M5. Initially, upon the rise of the WL, the intermediate node between these two NMOS transistors, Q!, is pulled up toward the precharge value of BL!. This voltage rise of Q! must stay low enough not to cause a substantial current through the M3-M4 inverter, which in the worst case could flip the cell. It is necessary to keep the resistance of transistor M5 larger than that of M1 to prevent this from happening. To keep the node voltage from rising above the transistor threshold (of about 0.4 volt), the cell ratio must be greater than 1.2 where cell ratio (CR) is defined by

$$CR = \frac{(W=L)\ 1}{(W=L)\ 5}$$

For large memory arrays, it is minimum sized, he access pass transistorM5 has to be made weaker by increasing its length. And pull-up ratio (PR) of the cell is defined by

$$PR = \frac{(W=L)\ 4}{(W=L)\ 6}$$

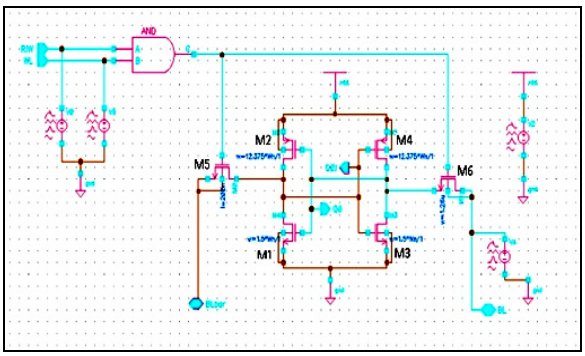

Figure 3.1.2: Schematic of The Circuit For 6 Transistor SRAM Cell

Which is lower than 1.8 to pull the node below VTn The lower PR, the lower the value of VQ.
CR = M1/M5 & CR > 1:2 Where M1= (W=L)1 = 1.5 and M5 = (W=L)5

$$M1=M5 > 1:2$$
$$M5 < M1=1:2$$
$$M5 < 1:25$$

And PR =M4/M6 & PR < 1:8 Where M4=(W=L)4 = 12.375 and M6 = (W=L)6

$$M4=M6 < 1:8$$

M6 > M4=1:8
M6 > 6:875

So, if W5 is 240 nm and L5 is 200 nm than (W=L)5 is 1.2 which is less than 1.25 and if W6 is
1260 nm and L6 is 180 nm than (W=L)6 is 7 which is greater than 6.875.

(W=L)5 = 240 nm / 200 nm = 1.2
(W=L)6 = 1260 nm / 180 nm = 7

Now as discussed the sizing of the transistors in 6T cell Ratio (CR) should be greater than 1.2 and pull-up ratio PR should be less than 1.8.

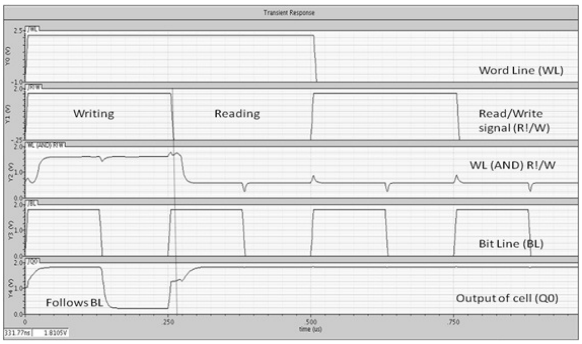

Figure 3.1.3: Transient Response For Reading And Writing Of The 6T Cell

Figure 3.1.3 shows the transient analysis of reading from the 6T SRAM cell and writing to the 6T SRAM cell. Transient analysis shows the waveforms for WL (word line), R!/W (read or write control line), BL (bit line) and output of the cell Q0. Here the frequency of the WL, R!/W and the BL is 1 MHz, 2 MHz and 4 MHz respectively. For reading operation R!/W is low and for writing it is high. So when R!/W is high writing operation is done and whatever the status of BL is writing to the cell and it appear at the output Q_0. Here for initial 500 ns WL is high and for 250 ns R!/W is also high. So during first 250 ns writing to the cell according to the status of BL is done. And after that only reading the status of cell is performed. Q0 is not change according to BL during reading.

4. SIMULATION RESULTS

Decoder With ATD Circuit for designing the decoder with ATD circuit, it is required to generate the pulse for every transition of each address and for that ORing of each address transition detection pulse is require and for that design of the NOR gate is required.

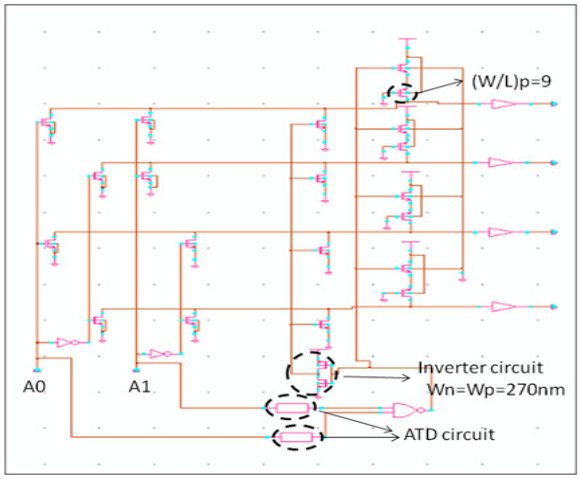

Figure 4.1.1: Schematic Of The Circuit For NOR-Based Decoder With ATD Circuit

Figure 4.1.1 shows the waveforms for the decoder with ATD circuit in which each address transition is detected by generating the pulses at every address transition. In the waveform of S0 + S1 of Figure 4.1.2, width of each pulse generated at the transition of addresses by ATD circuit is indicated in nano seconds. And for this duration of time periods the decoders inactivated, so that all the outputs of decoder are zero during that period of time. Because of the delay of ATD circuit at the output of the decoder two pulses are generated. One which has max voltage level less than the switching level of the buffer and one which has max voltage level greater than the switching threshold of buffer. So, by putting buffer pulse can be avoided which is of less Vmax level than the switching threshold of buffer. Figure 4.7 and Figure 4.8 shows the transient response of the decoder with ATD circuit for address transition period of 153 ns and 152 ns (frequency of 6.54 MHz and 6.58 MHz) respectively.

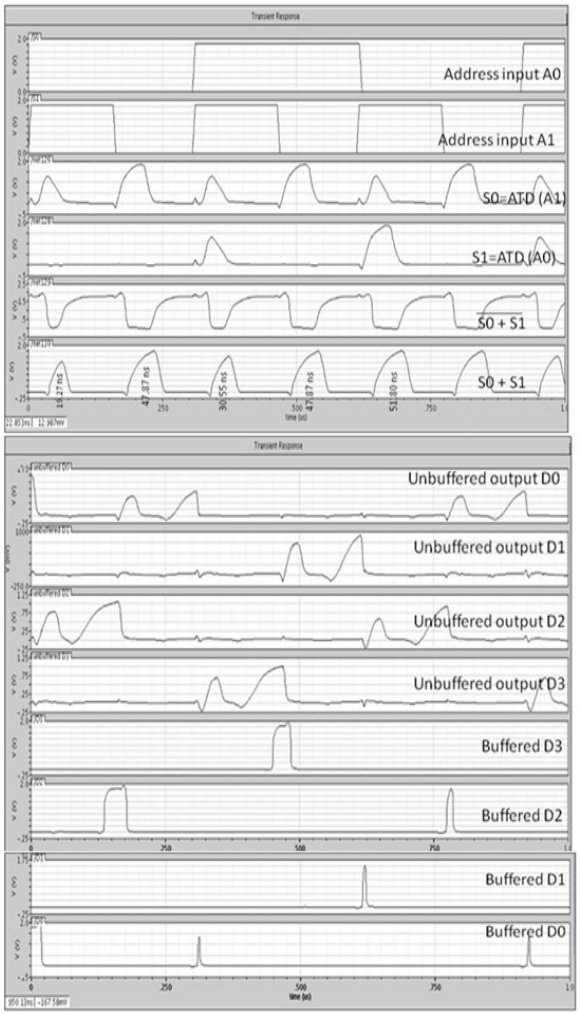

Figure 4.1.2: Transient Response For Decoder With ATD Circuit For Address Transition Frequency Of 6.54 MHz (T=153 ns)

SRAM without ATD Circuit

For designing the SRAM, ANDing of the decoder output with R/W signal is required and for that design of the AND gate is required which is discussed as given below.

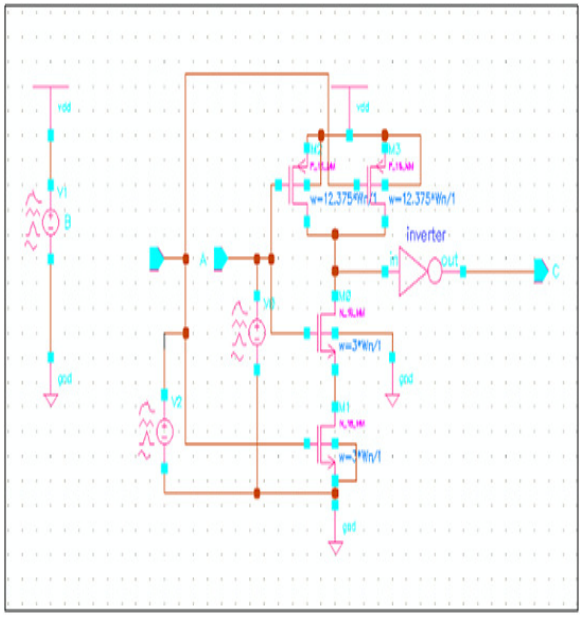

Figure 4.2.1: Schematic of The Circuit For AND-Based Decoder Without ATD Circuit

In AND schematic two pMOS is connected in parallel so the size of these both the pMOS (W=L)p is same as that of the inverter pMOS which is 12.375. And two nMOS is connected in series so size of both the nMOS (W=L)n is double than that of the inverter which is 2 * 1:5 = 3. Figure 4.9 shows the AND schematic in which the Wn = 180 nm. So, W/L ratio of each transistor is same as the multiplication factor with the Wn which is indicated besides each transistor

Figure 4.2.2 shows the waveforms for the SRAM without ATD circuit in which address A1 has noise which has the pulse width of 100 ns. This noise is decoded as a new address by the row decoder and it responds to this wrong address. And according to that corresponding output of the decoder D2 RD goes high which is generated due to noise. The R/W signal is high for the 1.9 ns so for that duration of signal writing operation is performed to the selected cell according to the status of BL.

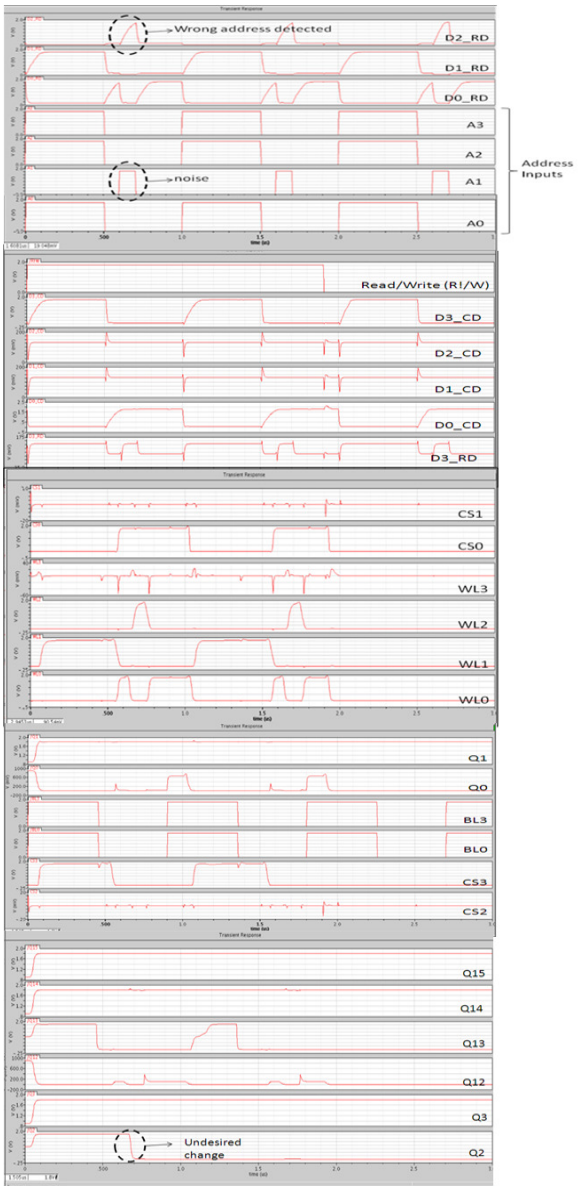

Figure 4.2.2: Transient Response for SRAM without ATD Circuit

5. CONCLUSION

In this work, an ATD circuit was designed to suppress the effect of noise on the address line in cadence virtuoso environment. The ATD circuit was sound to support a address change frequency up to 3.26 MHz. The testing was done on a 4*4 asynchronous SRAM core and the functionality of the circuit was successfully verified. The test circuit of 4*4 SRAM core was also designed in same environment. All the simulations were done for 180 nm technology node.

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