DESIGN OF VGA DISPLAY SYSTEM BASED ON CPLD AND SRAM

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***ABSTRACT** : VGA is Video Graphics Array and it is come in account in 1987. It displays approximate 256 simultaneous colors. Also it has 640 X 480=307,200 pixels maximum resolution. But with this resolution graphic card able to generate only 16 colors. This design is used to eliminate the use of CPU to display the textual data .The design will be developed using programmable logic device- based logic analyzer. And also it is used to combine video display controller with SRAM memory controller. And this design used to create a Video frame buffer. The SRAM should be 256Kx16 CMOS static ram memories. And these memories are used to store images that will be displayed on the VGA screen*

Now data from logic analyzer designed by other is combined to this design. Final goal is by using single chip CPLD and SRAM based logic analyzers which display the output measurement to monitor without interfaced to CPU. CPLD includes generation of VGA timing signal, finite state machine and logic control.

1. INTRODUCTION

The main intention of this design is to display an image into RAM, and onto a VGA monitor. This can be obtained by using an Xilinx XS95-108 board. This consists of the 32 KB SRAM and Xilinx XS9500 CPLD. This board is operated with 9 V power supply and it has 25 pins to download program. The VGA port is provided to connect to a VGA monitor. This port consists of 5 pins, Out of that, Two for TTL compatible signal, and three for colour (red, green and blue).

Generally to display the output on the monitor the logic analyzer uses C.P.U. But if we use such logic analyzer then there is problem of extra software that means it requires extra software for proper function. So by eliminating the use of CPU and to display the data on the monitor VGA display based on the CPLD and SRAM is necessary. With the help of such design data that gets from the controller in the SRAM is stores and then convert the data into analog signals to display on the VGA monitor. And all this operation is controlled by CPLD.

Before going to see system development of this design, we have to see its major component like, what CPLD is and which program downloading technique is used.

CPLD

CPLD (complex programmable logic device) is a device erasable programmable logic device that can be programmed with schematic and behavioural design CPLDs, which provides the features in between FPGA and PLAs. CPLD consist of number of circuits which contain series of gates and macro cells, each macro cell capable of implementing combinational and registered function. CPLD are ideal for complex box with large number of input. It require less board pace than FPGA, hence it has less board complexity than FPGA. In this design CPLD operates using its sampler module. This module is responsible to sampling appearance of the CPLD controller. CPLD also operate using Displayer module, this module takes care of the visuals of the oscilloscope.

VHDL

The 'V' stands for Very High Speed Integrated Circuit (VHSIC) and 'HDL' stands for Hardware Descriptive Language. VHDL is mainly dealing with the digital system. To verify the integrated system using single language VHDL is used. It is computer language used for formal description of the electronic device. VHDL is used to describe the circuit operation, its design, and tests to verify its circuit operation, also its basic concepts are analysis, elaboration, simulation, synthesis, test benches, interface, behavior and structure. In our design behavioral modeling is used. Behavioral modeling is used to describe the algorithm performed by the design. Behavioral modeling contains process statement, sequential statement, signal assignment statement. Whole functioning of VHDL depends on the input and output port.

2. SYSTEM DEVELOPMENT

To implement VGA system without Central processing unit then we have to use CPLD and PC based logic analyzer instead of CPU. If we generate VGA signal by using CPU then system requires extra software.

The basic building blocks of the design are synchronous counter with 25 MHz clock frequency, pixel RAM and Character-Generator ROM, and VGA signal generator.

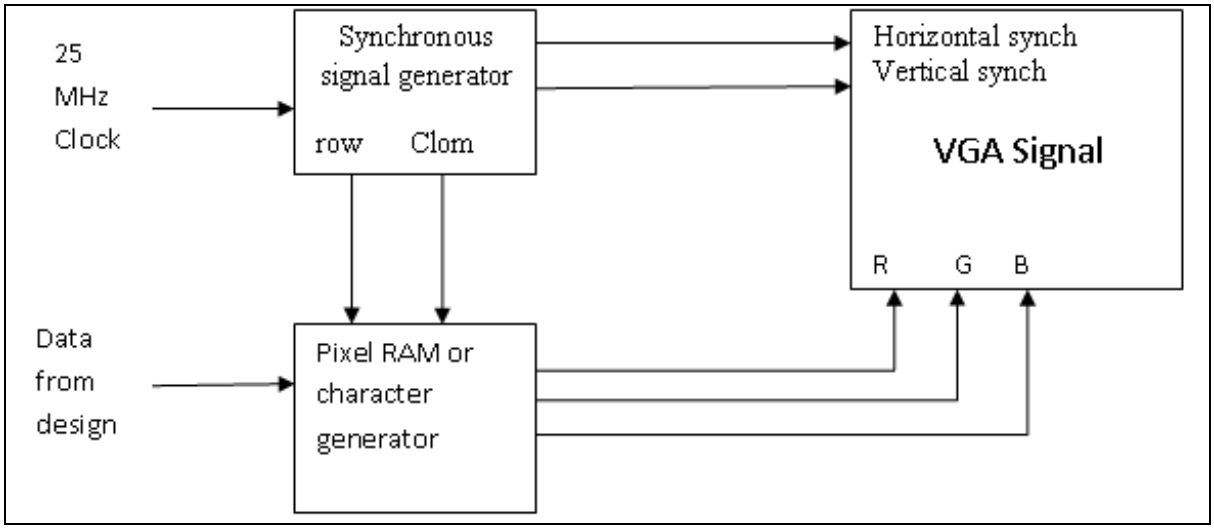

Figure (1): block diagram of VGA signal generator

To generate the VGA image with the help of CPLD and SRAM, we required VGA video signal. A VGA video signal consists of 5 analog signals. Out of that 5 signals two signals are TTL compatible signals, and remaining three signals are color signals, with 0.7 to1.0 V peak to peak voltage levels. These 3 signals are used to control the colures of VGA generator. The colour signals are RED, GREEN, and BLUE. And two TTL compatible signals are horizontal synchronous signal and vertical synchronous signal. These TTL compatible signals are used for video signal synchronization purpose. Circuit using resistor and diode is used to convert TTL output from the CPLD to the RGB signals for the video signal generation.

Red, Green, Blue signals combine known as the RGB signals. To generate number of colors using RGB signal, analog levels of these three signals are changes.

The face of the color CRT contains 3 different phosphors. One type of phosphor is used for each of the primary color red, green and blue. In standard VGA formats as shown in fig the screen contains 640 by 480 picture element or pixels. The video signal must redraw the entire screen 60 times per second to provide for motion in the image and reduced flicker. This period is called the refresh rate

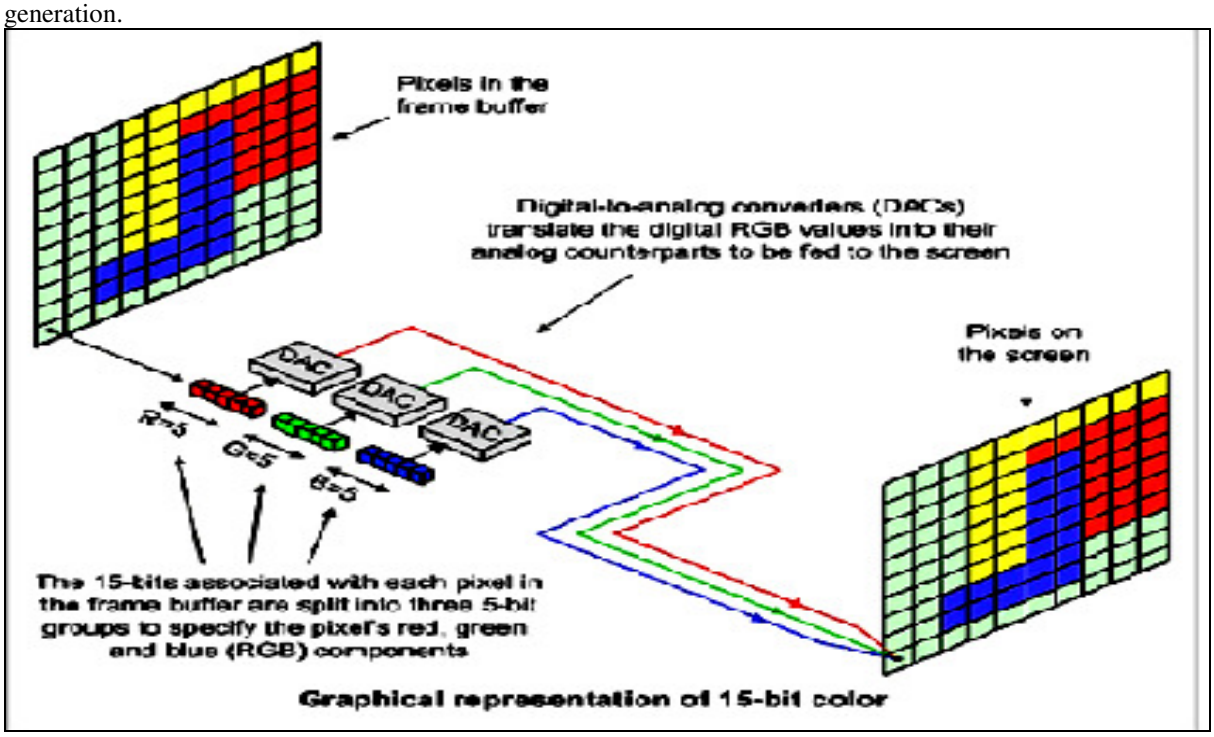

Figure 2: Pixel To Video

The human eyes can detect flicker at refresh rates less than 30 Hz. The vertical sync signal tells the monitor to start displaying a new image or frame ,and the monitor starts in the upper left corner with pixel 0,0.the horizontal sync signal as shown in fig(2) tells the monitor to refresh another row of 640 pixels. After 480 row of pixels are refreshed with 480 horizontal scan, the RGB signals should a be set to black color or all zero.

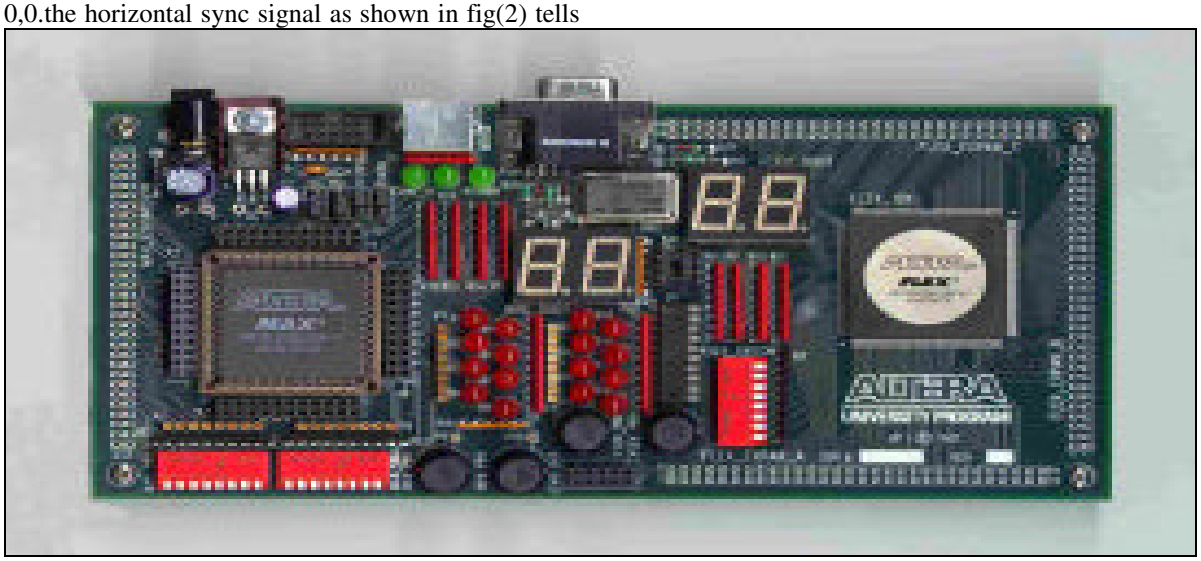

Figure 3: Altera CPLD Board

Many VGA monitors will shut down if the sync signals are not the correct values .Most PC monitors have an LED that is green when it detects valid sync signals and yellow when it does not lock in with the sync signals. In a PC graphic card, a dedicated video memory location is used to store the color value of every pixel in the display. This memory location is used to store the color across the screen to produce the RGB signals. There is not enough memory inside current generation CPLD chips for this approach so other technique will be developed which require less memory. To provide interesting output option in complex designs, video output can be developed using hardware inside the CPLD or FPGA.

A good example is where a CPLD is where a CPLD is used to load configuration data for an FPGA from non-volatile memory CPLDs were an evolutionary step from even smaller devices that preceded them, PLAs and PALs.

The most important part of this project is the timing of writing to the monitor. If the horizontal timing and the vertical timing are not synchronized then nothing will be displayed on the screen. That is why there is a horizontal synchronization signal and a vertical synchronization signal. The essential process is that the horizontal signal will write one line of pixels on the screen, and then enter a blanking period in which it pulses low. This pulse is to notify the vertical signal that the horizontal signal is at the end of the line and needs to move down to the next row. When the vertical signal reaches its blanking time at the bottom of the screen it pulses low to notify the horizontal signal that it is at the bottom and that they should both return to the top left hand corner of the screen to begin writing again. There are specific times for these pulses to occur and for the writing of the screen to occur. The so called blanking period is extra time outside of the visible region of the monitor at the end of each horizontal and vertical signal count this time is used for any calculation's or changes in information because if things like calculations are done when the process is writing to the monitor errors and confusion can occur. The actual measurements for the timing are based on the time the circuitry within the monitor needs to write to the screen properly. A very good picture of the timing of the horizontal and vertical signals can be found on page 3 of VGA monitor manual found on the XESS website at the XS95 Displaying a VGA Signal Manual. The timing simulation diagram below shows a simulation of the actual tester program that was used. It depicts only a part of the timing diagram. It would take pages to show the full time it takes to write out the signals to the entire visible and non-visible region of the screen. The important signals to look at are vsyncb, hsyncb, oeb, and rgb.

vsyncb: Is high on this portion because we are writing one horizontal row of pixels. It will go low for a pulse period when we are at the bottom of the visible region of the screen.

hsyncb: At around 59 us, the hsyncb pulse goes from a high to a low. At this time we have gone beyond the visible region of the screen and finished writing the line. It is pulsing low for a time period to indicate this and to co-ordinate with the vertical timing.

oeb:This signal is the read signal from the RAM chip. While it is low, we are reading from the RAM and producing and output on the screen (see the RGBsignal). When it goes high, we stop reading from the RAM because we are at the end of the line and do not need to read anything.

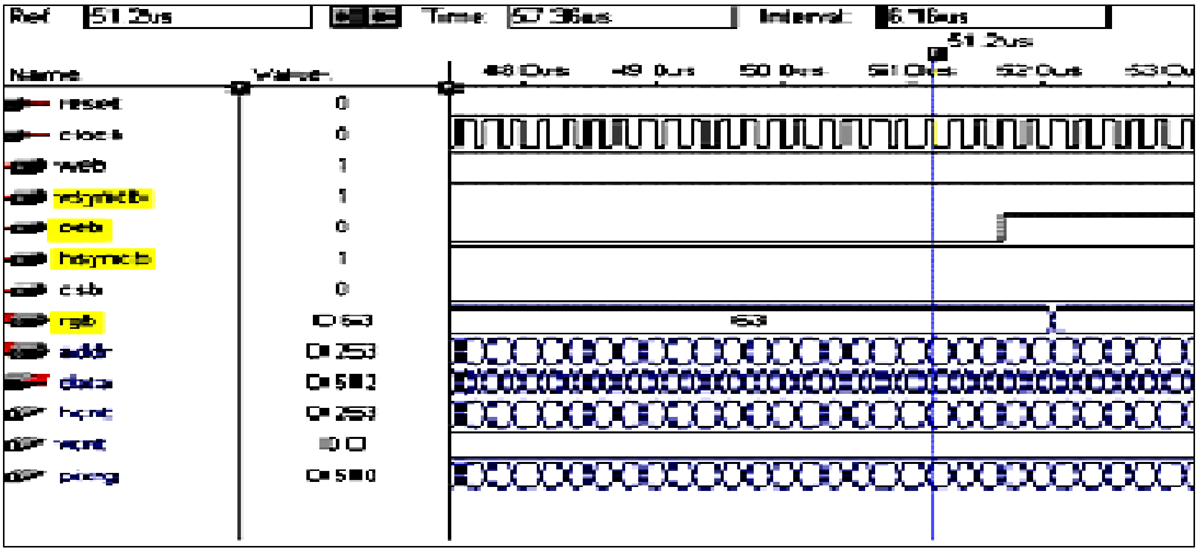

Figure 4: Timing Simulation of Major Signals

RGB: on this section, the color being displayed on the screen is red. Further along in the timing, you would see this color changing. You can also see that it goes to 0 when oeb is enabled because we are in the non-visible region.[2]

2.2 VGA with SRAM

In the middle of the VGA display create an array of16 by 16 color blocks for a total of 256 blocks. Each block should be 32 pixels wide by 16 pixels deep. The color of each of the blocks to be displayed should be read from the bottom 256 bytes of the SRAM. The value to be stored in the SRAM locations should increment from 0x00 at address location 0x00 to 0xFF at address location 0xFF. The value of0x00 should represent black and a value of 0xFF should represent white, with the different colors in between. [2].

3. CONCLUSIONS

Most of the logic analyzer uses C.P.U. to display the output on the monitor. The problem of existing logic analyzer is that it requires software in order to function properly. Furthermore it is not portable. Hence to eliminate the use of CPU to display the data on the monitor VGA display based on the CPLD and SRAM is necessary. As a video image display interface standard, VGA interface has been widely used in the embedded system. Due to the lack of professional VGA display controller in most embedded systems, splash screen, even blank screen problems may appear while displaying the high-resolution video image. The design illustrates the implement method of VGA display controller, which combines CPLD and SRAM. First, the design stores data that gets from the processor in the SRAM and then reads them out in form of VGA display interface standard into D/A converter which will convert the data into analog signals to display. The whole operation above is controlled by CPLD. So such a design can effectively solve the problems caused by insufficient bandwidth in the displaying, what's more, it can reduce the pressure of the CPU.

4. ADVANTAGES

1. Using VGA, the signal from the CPU is converted to VGA by the video adapter and sent to a monitor with VGA input.
2. VGAs provide are More Secure Signal.
3. It provides stronger connections. Also have to deal with interruptions.
4. Another advantage of having a VGA cable is that the quality of the videos is going to be drastically improved. With them, we didn't receive blurry images or videos in really poor resolution.

5. DISADVANTAGES

1. It not operated with Fewer lanes with embedded self-clock, reduced EMI with data scrambling and spread spectrum mode
2. Does not support to easy expansion of the standard with multiple data type
3. Also does not support to High resolution displays and multiple displays with a single cable.
4. Not work for internal chip-to-chip communication

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7. REFERENCES

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