# ANALYSIS AND DESIGN OF A 3.1–10.6 GHZ WIDEBAND LNA IN 130-NM CMOS TECHNOLOGY

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***ABSTRACT****- This paper presents a wideband low-noise amplifier (LNA) based on the cascade configuration. Wideband input-impedance matching was achieved. While the wideband gain response was obtained using a post-transistor inductor. Theoretical analysis shows that the frequency response of the power gain, as well as the noise figure (NF), can be described by second-order functions with quality factors or damping ratios as parameters, Implemented in 130 nm CMOS Technology. This achieves S11 below 10 dB, S22 below 10 dB, flat S21 of 22dB, and flat NF of 4.45dB over the 3.1–11.6GHz band. The analytical, simulated, and measured results are mutually consistent*

***Keywords—CMOS, Feedback, Flatness, Low-Noise Amplifier,(LNA), Matching, Noise Figure (NF), Series Peaking, Wideband.***

## I. INTRODUCTION

RECENTLY, wideband technology has attracted much attention because of its high data-rate transmission capability. In such a wideband system, a low-noise amplifier (LNA) with wideband input-impedance matching is a must. The need to reduce the size, cost and power consumption of portable electronics is the driving force behind the motivation to integrate RF front-end and digital signal processing on a single chip. CMOS technology is the most attractive solution due to the low cost, high density and high performance in terms of speed. Typically, high gain and low noise in LNAs involves high power dissipation, which is not desirable in portable electronics. At high frequencies, CMOS LNAs typically have signal loss through the drain/source to substrate parasitic which degrades the NF and power gain.

In some applications broadband is not required, therefore to reach this goal, various wideband-matching techniques for wideband LNAs have been proposed. For example, a cascade CMOS LNA with a band pass response at the input for wideband impedance-matching has been reported. Such topology incorporates the input impedance of the cascode amplifier as a part of the filter. However, the adoption of the filter at the input requires a number of reactive elements, increasing die-size and the noise figure (NF) due to the finite quality (Q) factor of the passive components when implemented on-chip. Alternatively, broadband matching with low power dissipation and small die size can be realized by common-gate input topology. Nevertheless, a single-stage common-gate amplifier cannot provide sufficient power gain, and hence, extra stages are required to boost the gain, resulting in ripples in the pass band due to non-broad band inter-stage matching. In another work, a noise-cancelling technique was introduced to resolve the high NF issue arising from the common-gate amplifier. However, according to the experimental results, the achieved NF was still high, even higher than that of the LNAs without the use of noise cancelling. Although the distributed amplifier (DA) has the inherent advantages of wideband impedance matching and gain, it is notorious for its low gain, high power dissipation, and large chip area. Resistive feedback was adopted to reduce the factor of the input series circuit to achieve wideband impedance matching. However, the impedance/gain bandwidth of this design was still limited due to the non-optimized choice of the factor of the input network and the large capacitive effect from the active devices. Notably, while the frequency responses of gain can be very flat, the frequency responses of the NF are not flat in most of the published wideband LNAs because there is an intrinsic conflict between flat gain and flat NF responses.

## II. OVERVIEW

Figure 1 shows the set of variables that affect LNA performance. It is up to the designer to impact of environmental variables, while finding the most appropriate trade−off between competing characteristics to optimize receiver sensitivity and selectivity, and maintaining information integrity. Low noise amplifiers (LNAs) play a key role in radio receiver performance. The success of a receiver's design is measured in multiple dimensions: receiver sensitivity, selectivity, and proclivity to reception errors. The RF design engineer works to optimize receiver front−end performance with a special focus on the first active device. To illustrate the practical challenges, performance trade−offs for three popular LNA topologies and two process technology

implementations are examined. Five characteristics of LNA design are under the designer's control and directly affect receiver sensitivity: noise figure, gain, bandwidth, linearity, and dynamic range. Controlling these characteristics, however, requires an understanding of the active device, impedance matching, and details of fabrication and assembly to create an amplifier that achieves optimal performance with the fewest trade−offs.

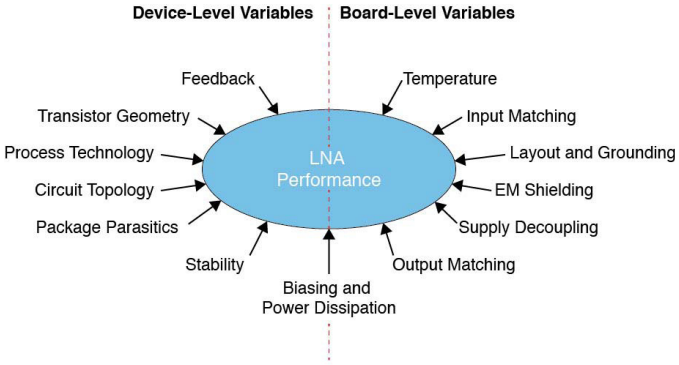


Figure1. LNA Performance Variable

## III. LNA TOPOLOGIES

Common−source, common−gate, and cascode are three prevailing LNA topologies. Table 2 provides a concise comparison based on the most relevant considerations for LNA design.

| Characteristic | Common−Source | Common−Gate | Cascode |
|---|---|---|---|
| Noise Figure | Lowest | Rises rapidly with frequency | Slightly higher than CS |
| Gain | Moderate | Lowest | Highest |
| Linearity | Moderate | High | Potentially Highest |
| Bandwidth | Narrow | Fairly broad | Broad |
| Stability | Often requires compensation | Higher | Higher |
| Reverse Isolation | Low | High | High |
| Sensitivity to Process Variation, Temperature, Power Supply, Component Tolerance | Greater | Lesser | Lesser |

Table1. Comparison Three LNA Topologies

The cascode amplifier is the most versatile of the three topologies. It provides the most stable signal gain over the widest bandwidth with only a slight sacrifice in noise figure performance and design complexity. The common−source transistor is sized to deliver the best possible noise figure, but that advantage often comes at the cost of greater sensitivity to bias, temperature, and component tolerances. The raw transistor rarely has its Yopt coincide with Yin. To minimize the need for external noise matching circuit components, the LNA designer manipulates transistor construction (gate finger multiples, finger dimension, interconnects, and layout), RF feedback, and package parasitics to have Yopt simultaneously converge on Yin and the system's characteristic admittance.

Careful insertion of source degeneration feedback also improves amplifier stability and linearity at the expense of gain, especially at higher frequencies. Too much or too little feedback, however, degrades stability and performance; therefore, the LNA designer seeks the optimal value. This design feature allows the user to find a much better trade−off between amplifier noise figure, gain, and input return loss.

The cascode amplifier combines the common−source stage previously described with a common−gate transistor designed for optimal linearity. The cascode amplifier, however, becomes greater than the sum of its parts when the common−source transistor is also designed to pre−distort the common−gate transistors. These design features greatly ease LNA implementation and improve stability, bandwidth, and linearity.

## IV. BIAS BIASING NETWORK DESIGN

Setting the LNA bias is the first most critical step in implementation. Most LNA MMICs have an integrated active−bias circuit that regulates bias currents over variations in supply voltage, temperature, and FET threshold voltage. Careful selection of a bias point, however, is still required to find the best compromise between gain, NF, and linearity for any given application. There are several important considerations when approaching the task of input matching. Noise figure degradation can be mitigated by limiting the number of elements between the antenna and LNA input. A high−Q input matching network provides an optimal noise figure and gain performance because of the minimal loss, but these networks are often quite sensitive to variations in process, voltage, temperature, and component value.

## V. INPUT AND OUTPUT MATCHING

Careful design produces a device with well–controlled input and output impedances at which the optima of various important performance characteristics come close to coinciding. There are several important considerations when approaching the task of input matching. Noise figure degradation can be mitigated by limiting the number of elements between the antenna and LNA input. A high–Q input matching network provides an optimal noise figure and gain performance because of the minimal loss, but these networks are often quite sensitive to variations in process, voltage, temperature, and component value. There are a number of performance parameters that show to what extent the impedances are matched. Firstly, the Reflection Coefficient which by definition is the ratio of the reflected wave to the incident wave (Equation 1.), but can also be expressed in terms of impedances. It is a complex entity that describes not only the magnitude of the reflection, but also the phase shift.

$$\Gamma_L = \frac{Reflected\ wave}{Incident\ wave} = \frac{Z_L - Z_S}{Z_L + Z_S} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

This is the load reflection coefficient with respect to the source impedance. It is also commonly expressed with respect to the characteristic impedance (Z0). When the load is short-circuited, maximum negative reflection occurs and the reflection coefficient assumes minus unity. In contrast, when the load is open-circuited, maximum positive reflection occurs and the reflection coefficient assumes plus unity. In the ideal case, when ZL is perfectly matched to ZS, there is no reflection and the reflection coefficient is consequently zero. A closely related parameter is the Voltage Standing Wave Ratio (VSWR). The VSWR is defined as the ratio of the maximum voltage to the adjacent minimum voltage of that standing wave (Equation 2). Knowing the domain of the reflection coefficient, it follows that when there is no reflection as in a perfectly matched system; VSWR assumes its minimum and ideal value of 1.

$$VSWR = \frac{|V|_{max}}{|V|_{min}} = \frac{1 + |\Gamma_L|}{1 - |\Gamma_L|} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The source- and load impedances are fixed; the objective is to design the input matching network so that ZS matches Z1 and the output matching network so that ZL matches Z2. In other words Z1 and Z2 respectively, are transformed to perceptually match the input and output impedances of the transistor. According to the Maximum Power Theorem, the maximum power transfer will occur when the reactive components of the impedances cancel each other, that is when they are complex conjugates. This is suitably called conjugate matching.

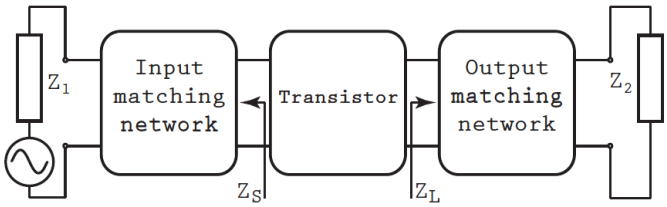


Figure2. Matching network in microwave amplifier.

To achieve the conversion with an impedance matching network of passive components, there are primarily three options. Firstly, there is the L-match. Its advantage is the simplicity, but that is simultaneously its downside as well because it has only two degrees of freedom. Since there are only two component values to set, the L-match is restricted to determining only two out of the three associated parameters: impedance transformation ratio, center frequency and Q. To acquire a third degree of freedom, it is therefore desired to cascade another L-match stage. By doing so, another two types of impedance transformation matches are encountered: the π-match and the T-match.

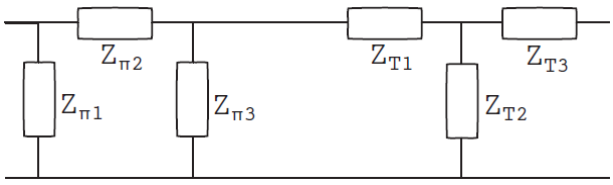


Figure3. Cascade π match and T match network.

The advantages with the T- and π-match configurations do not end with an additional degree of freedom. But because of their topology they can absorb parasitic reactance present in source or load. Specifically the T-match will absorb parasitic inductance whereas the π-match will absorb parasitic capacitance. In addition it is also

possible to achieve significantly higher Q compared to an L-match configuration. Another noteworthy impedance transformation option is band pass filtering where the port impedances are unequal.

## VI. SCATTERING PARAMETERS

Scattering Parameters or S-parameters are complex numbers that exhibit how voltage waves propagate in the radio-frequency (RF) environment. The characteristics of the 2-port is represented by a set of four S-parameters: S11, S12, S21 and S22, which correspond to input reflection coefficient, reverse gain coefficient, forward gain coefficient and output reflection coefficient respectively. S-parameters, on the other hand, are measured under matched and mismatched conditions. Under such circumstances, it becomes necessary to measure the parameters.

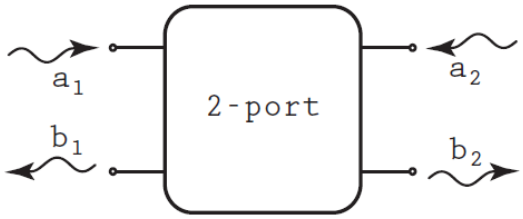


Figure4. A two port with incident wave's a1 & a2 and reflected waves b1 & b2

Referring to Figure 4, these measurements are carried out by measuring wave ratios while systematically altering the termination to cancel either forward gain or reverse gain according to the following equations:

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0}, \quad S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0}, \quad S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0}, \quad S_{22} = \frac{b_2}{a_2}\Big|_{a_1=0}.$$

$$b_1 = S_{11}a_1 + S_{12}a_2, \quad b_2 = S_{21}a_1 + S_{22}a_2.$$

## VII. THE QUALITY FACTOR

The Quality Factor (Q) is a descriptive parameter of the rate of energy loss in complete RLC networks or simply in individual inductors or capacitors. For the latter, Q is a measurement of how lossy the component is, that is how much parasitic resistance there is. So it follows that in applications where loss is undesirable, high Q components are advantageous. The equations for calculating Q are:

$$Q_{RLC} = \omega\frac{E_{tot}}{P_{avg}}, \quad BW = \frac{\omega_0}{Q_{RLC}}, \quad Q_L = \frac{X_L}{R} = \frac{\omega L}{R}, \quad Q_C = \frac{|X_C|}{R} = \frac{1}{\omega CR}.$$

## VIII. CIRCUIT DESIGN

Figure 4 shows a two-stage WLNA is employed to simultaneously achieve a high gain and a wide band. The proposed UWB LNA consists of a π-match filter, to achieve a low NF over a wide band, the channel noise of MOS and the input matching network must be considered. The channel noise is related with a γ-factor, the process parameter of which depends on the bias condition, that is, the gate-source voltage Vgs and transconductance (gm). Therefore, the noise contributed by M1 can be minimized by considering its gate width and bias current. Simulation with Agilent's Advanced Design System (ADS) produced an optimized M1 with a width of 30μm, a gate bias Vg1 of 0.84 V, and a drain current of 8.6 mA.

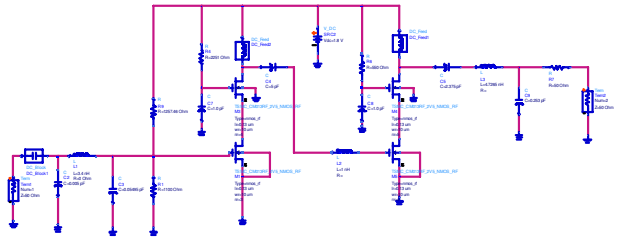

Figure5. Shows the complete schematic circuit of 3.1-10.6 GHz a cascade Low noise amplifier.

L is kept to its minimum; VGS and W are key design parameters that directly link to power consumption. Drain-to-source voltage, the performance of the MOSFET is strongly tied to the drain current density ID/W, which can only be modified by VGS but not by W. The LC filter impedance matching method is applied to input and output ports for higher integrating level. At last, an inductor is applied to the source of the transistor to accomplish the impedance matching and noise matching by the same time. The measurement result shows good

performance on noise figure and VSWR. An important character of this structure is that it shows quite high output impedance comparing with CS LNA.

## IX. Simulation Results And Measurment

It is simulated using Advanced Design System (ADS) 2009. The simulation recorded that the amplifier gain S21 is 26dB. The input return loss S11 is -16dB, overall noise figure (NF) is 4.4dB and the output return loss S22 is -8.5dB.The reflection loss S12 is -86dB. These values were within the design specification and were accepted. The outputs S-parameter are shown below.

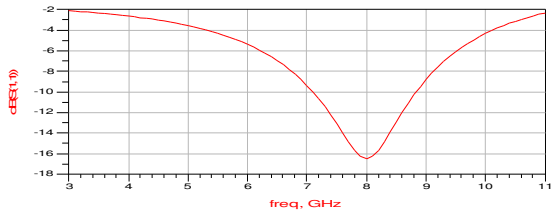


Figure6. Input Reflection Coefficient


Figure7. Output Reflection Coefficient

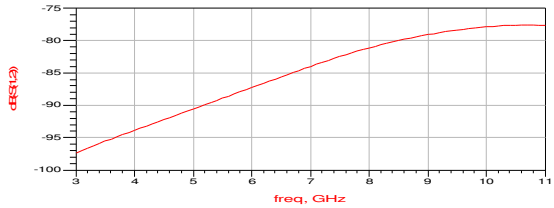


Figure8. Reverse Isolation

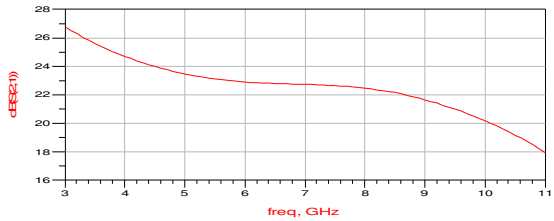


Figure9. Power Gain

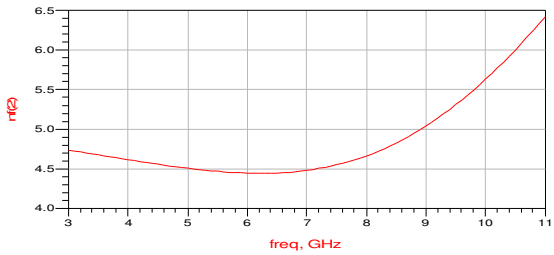


Figure10. Noise Figure

## X. CONCLUSION

The 3.1-10.6GHz LNA has been developed successfully and the circuit contributed to the front end receiver at the described frequency. For better performance in gain of the amplifier, it can be achieved by increasing the number of stages to improve the gain and noise figure of the design. Higher gain would expand the coverage or communication distance. WLNA designed using 130nm CMOS process. The LNA applies cascade structure with source inductive degeneration technology. The π-match filter method is applied for impedance matching. A resistor voltage divider circuit is used to supply DC self-bias voltage.

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