JOURNAL OF INFORMATION, KNOWLEDGE AND RESEARCH IN
ELECTRONICS AND COMMUNICATION (ISSN 0975 – 6779 , GIF: 01.6890 – SIF: 02.885)

A Review on FFT ASIP Architecture Design for OFDM System

Er.Adityaprakash N. Sharma
M.Tech (Digital Communication)
Lecturer (G.H.Raisoni Polytechnic, Nagpur
E-mail Id.ap.sharma07@gmail.com/9921344851

Abstract: **The Fast Fourier transform (FFT) has presently a key role in signal processing applications. Most of the system needs high flexibility, high speed and high efficiency. The baseband hardware should be economical and capable enough to compute FFT within the time constraints necessary to support multiple wireless standards. Baseband hardware should be scalable so it supports multiple wireless standards as well as it should meet the performance constraints such as high speed, low area and low power consumption. Hence, the baseband hardware needs a scalable FFT module that meets the performance constraints required by multiple wireless standards. This paper presents a highly efficient hierarchical design of an application specific instruction set processor architecture exploration, software tools design, system verification and design implementation. Simulation and synthesis results show that our FFTASIP achieves a higher energy-efficiency and flexibility and the area cost will be low.**

Keywords: Application-specific instruction set processor (ASIP), fast Fourier transforms (FFT), hierarchical design, sparten kit, code composer, and radix.

1. Introduction

The wired telecommunication networks provide low-bit-rate services as well as high-bit-rate services. Voice services need low-bit-rates whereas broadband transmission services need high-bit-rates. Wireless communication networks additionally give the desired services. However, some of the high-bit-rate services are restricted due to various performance constraints. During the course of time, there has been a growing demand for high-bit-rate services in wireless communication systems. Fast Fourier Transformation (FFT), the most time intense block in electronic communication systems, is facing both high flexibility and throughput requirements in current high speed wireless systems. It should be simply reprogrammed or reconfigured to support various standards and operating modes. For instance, the scale of FFT is desired to be changeable under different operation environments. The existing application-specific integrated circuits (ASICs), although can provide high throughput, cannot provide the desired flexibility and programmability. On the other hand, high throughput is important for FFT computation as well. The fast Fourier transform (FFT) and inverse FFT (IFFT) algorithms are core processing blocks used for conversion from time-to frequency domain (FFT) and from frequency-to-time domain (IFFT) and represent the most computation intensive tasks. The proposed FFT ASIP designed can have both high computation similarity and low memory access based on a hierarchical array structure. It will adopt the epoch idea, splits an N point FFT into two smaller FFT loops, then reconstruct the inner-loop FFT data flow into an array structure. The structure contains a set computation module. The proposed design extends the basic processor core with the computation module and adds custom register files to store all the intermediate results of the inner-loop FFT computations. The efficient addressing methods for each data and coefficients, which may remove the address changing logic

2. LITERATURE SURVEY

The transceiver of OFDM with respect to standards of IEEE 802.11 had been implemented and discussed by Nagaraju et al (2012) to optimize the factors – power and time. The blocks of transmitter and receiver were synthesized without the help of a decoder. The concepts of Quadrature amplitude modulation and Convolution were used to improve the bandwidth and data rate respectively. Generally an OFDM is realized using a FFT processor having individual clocks for modulation or demodulation to improve the overall data rate. The principle of clock scheduling was used to meet the constraints in time. The parameters - threshold voltage and clock gating were adopted to reduce the consumption of power. This design had been implemented using standard 0.18 μm technology with the specifications - chip size was 5.76 mm^2, power consumption was 72 mW at a volatge of 1.8 V. This design obtained significant improvement in gain and data rate when compared to traditional Wireless Local Area Networks.

Hidalgo *et al* (1999) presented an architecture of FFT, smaller in area that adopted the principle of constant-geometry. It comprised a group of processors connected to each other by a means of an unshuffle network. Each processor in the group had an individual memory, one read port and write port for the transformation 'N' of size 'D' with 'P' number of processors. The read and write ports, read 'r' number of butterfly inputs and write 'r' number of temporary results respectively. The circuit meant for generation of addresses was simple and the design architecture decreased the area by 50% approximate when compared to other designs.

2. PIPELINED FFT PROCESSORS

The FFT processor is an inevitable component used for implementing the systems of OFDM. The pipeline architectures in structured form are adopted to satisfy the requirements of energy and signal processing as far as mobile environment is concerned. The architectures of FFT based on decomposition method and radix-2^i algorithm were proposed by **He** *et al* (1998). The algorithm was exploited for the implementation of dominant elements to decrease the count of manipulations and the storage capacity. The storage capacity had been optimized by adjusting the word length in a progressive manner. The efficiency of the design with respect to area and power was improved by using a multiplier based on distributed arithmetic. The specifications of the design were obtained by using a 1024 point FFT processor.

Song-Nien Tang *et al* (2012) proposed a FFT processor for various types of wireless networks such as wireless LAN, wireless MAN etc. By adopting the Flexible-Radix Configuration Multiple Delay Feedback (FRCMDF) commutator, a high performance could be obtained by FFTs of variable-length in an efficient manner. In order to improve the efficiency with respect to area and energy, an optimized method of multiplication was also suggested. In addition, the architecture could provide a support for scaling the power across the modes of FFT. The chip had been realized with a size of 3.2 mm^2, a signal to noise ratio of 40 dB, power consumption of 507 mW at 300 MHz. This FFT processor of length 512-point was able to give higher performance and lower consumption of power when compared to other designs.

Taesang Cho (2013) presented a radix-2^5 fast Fourier transform (FFT) processor of length 512-point for applications of personal area wireless networks. A modified version of radix-2^5 algorithm of FFT was used to decrease the level of hardware required. This technique could decrease the count of manipulations and the capacity of memory required. A complex multiplier was employed in the place of a Booth multiplier. The architecture obtained a SNR value of 35 dB with a word length of '12' bits at 1.2 V. This design had been implemented using 90-nm technology with the specifications - gate count was 2, 90, 000, the rate of throughput was 2.5 Gigabits per second at 310 MHz.

Kyung Heo et *al* (2003) proposed a FFT processor using mixed radix algorithm and a new in-place technique. This processor employed only two numbers of N-word memories for implementation of FFT when compared to existing FFT processors which employ four numbers of N-word memories. Further this architecture obtained the optimum

requirements with respect to area and signal processing. The number of clock cycles and number of gates were 640 and 37, 000 respectively for a FFT processor of length 512-point. Hence this design could reduce size of memory and gate count when compared to other FFT processors.

Shousheng He *et al* (1998) discussed a FFT processor of length 1024-point using pipeline architecture. This architecture utilized the regularity of radix-2^2 FFT algorithm. The implementation of FFT processor was obtained with only four numbers of complex multipliers and a data memory of 1024 points. The chip had been realized with 0.5 µm CMOS technology with an area of 40 mm^2 at a frequency of 30 MHz.

Han Ying *et al* (2003) introduced a FFT processor based on Xilinx FPGA. To reduce the complexity of logic, the serial mode was adopted to subject the data into three operations such as inclusion of multiplying window, manipulation of FFT and computation of module-square. The frequency of the clock was increased to obtain better performance by employing the serial and parallel architectures thereby avoiding the bottleneck. It was shown that the processor obtained high performance and was suitable for applications of Digital signal processing.

Chang *et al* (2003) presented an architecture based on algorithm of Radix-4. By integrating the styles of feed forward and feedback commutators, this architecture obtained better usage of hardware and memory when compared to other FFT processors. Moreover various components of ROM were needed for storing the twiddle values. The size of ROM was decremented by an integer of '2' using the concept of redundancy. The single-frequency networks are constructed on a large scale using Coded Orthogonal Frequnecy Division Multiplexing (COFDM) system, with appropriate guard durations to make the echoes invalid. The fast Fourier transforms of longer length have to be implemented for demodulating every symbol in order to reduce the losses of spectral efficiency to about 20%.

Petrovsky *et al* (2006) proposed a technique for synthesizing the split radix FFT processors using pipeline architecture. This technique was adopted using hardware design of FPGA by considering the constraints of practical applications such as frequency, length of transform, performance etc into account. The illustrated examples of architecture showed the abilities of the technique to optimize the hardware. The transition from variable arithmetic to fixed arithmetic along with appropriate issues of accuracy was also discussed.

Yang *et al* (2013) proposed FFT architecture of variable length using multiple delay commutator for MIMO-OFDM systems. In this design, radix-N butterfly elements were employed at each stage. Because of this, complete utilization in elements of computation was obtained. Moreover the simple memory methods of scheduling were used for ordering the input and output bits. This accounted in improvement of utilization rate for usage of memory. Since the requirements of memory generally excel the die area in FFT processors, appropriate reduction in size of memory and die area in this architecture could be achieved in an effective manner.

Kirubanandasarathy *et al* (2010) proposed a Fast Fourier Transform (FFT) processor using pipeline architecture for applications of MIMO OFDM. The required parameters - high performance, low power and reduction in memory were obtained by employing mixed radix FFT 4/2
with bit reversal in the architecture.

Shuenn-Yuh Lee *et al* (2006) proposed a memory architecture using mixedradix FFT. A simple circuit for the generation of memory addressing was provided. The sequence of butterfly elements in mixed-radix was produced by means of a timer in an automatic manner. In this processor, the coefficients of size N/8 were saved thereby reducing size of ROM and the area of processor. In addition,

3. Proposed Work

1) Firstly adopting the epoch idea splits the N- point FFT into two or three small FFT loops depending on the number of points.
2) The structure contains a fixed computation module, which is an 8 point radix 2 butterfly unit. The butterfly unit is uniform stage-independent basic

structure, reducing the processing complexity and simplifying the data addressing method

3) Uses TMS320C6X processor as a platform, extending the basic processor core with the computation module and adding custom register files to store the intermediate results within the inner loop FFT computation.
4) Propose efficient addressing methods for both data and coefficients.
5) Customize the instruction set
6) With the support of an array structure and efficient data addressing logic, the FFT algorithm can be scaled for any size of computation.

4. SUMMARY

Research papers and articles published in leading Journals, related to implementation of efficient pipelined FFT processors for OFDM applications were collected and the important findings were critically reviewed. From the above review, it is understood that many researchers all over the world are carrying out investigations on pipelined FFT processors to understand the impact of power, area and complexity of hardware against the performance of the processors. Moreover, there are no much literature available relating to the implementation of 128 point pipelined FFT processors for OFDM applications. Keeping the above facts in mind, the present investigation was carried out.

5. Conclusion

This paper will proposed a hierarchical radix 2 FFT ASIP design, which will be flexible and efficient to meet the requirements of contemporary digital communication standard. And also provide high throughput computation parallelism and low memory access based on a hierarchical array structure. The hierarchical array structure offers good scalability to any point FFT, and both hardware and software are easy to implement. The cost, area and power consumption will be acceptable.

References

[1] Wei Hun,Erdogan, Arslun, and M. Hasan, "The Development of High Performance FFT IP Cores through Hybrid Low Power Algorithmic Methodology,"2005IEEE. Pp.549-552.

[2] Ramesh Chidambaram, Rene van Leuken Marc Quax, Ingolf Held, Jos Huisken, "A Multistandard FFT Processor for Wireless System-on-Chip Implementations 2006 IEEE.pp.1099-1102

[3] Adnan Suleiman, Hani Saleh , Adel Hussein, and David Akopian, "A Family of Scalable FFT Architectures and an Implementation of 1024-Point Radix-2 FFT for Real-Time Communications," 2008 IEEE PP-321-327

[4] Relationship 4. Xuan Guan, YunsiFei, and HaiLin,"A Hierarchical Design of an Application- specific Instruction Set Processor for High-throughput FFT," 2009 IEEE.pp.2513-2516.

[5] Yazan Samir Algnabi 2Furat A. Aldaamee, 3Rozita Teymourzadeh, 1Masuri Othman and 1Md Shabiul Islam , " Novel Architecture of Pipeline Radix 22 SDF FFT Based on Digit-Slicing Technique" 2012 IEEE PP-
470-474

[6] XuanGuan,YunsiFei and Hai Lin, "Hierarchical Design of an Application-Specific Instruction Set Processor for High-Throughput and Scalable FFT Processing," March 2012 IEEE. VOL. 20, NO. 3, pp.551-563.

[7] Shang-Ho Tsai, Kai-Jiun, "MDC FFT/IFFT Processor With Variable Length for MIMO-OFDM Systems" IEEE , VOL. 21, NO. 4, APRIL 2013

[8] Ho Yang, NavneetBasutkar, PengXue, Kyeongyeon Kim, and Young-Hwan Park,"Software-Defined DVBT2 Demodulator using Scalable DSP Processors IEEE Transactions on Consumer Electronics, Vol. 59, No. 2, May 2013 pp.428-434

[9] ManoharAyinala, Yingjie Lao, Student Member, IEEE, and Keshab K. Parhi, Fellow, An In-Place FFT Architecturefor Real-Valued Signals IEEE Transaction on circuits and system-II, VOL. 60, NO. 10, OCTOBER 2013 pp.652-656

[10] Ting Chen1a, Xiaowei Pan2, Hengzhu Liu1, Tiebin Wu11,"Rapid Prototype and Implementation of a HighThroughput and Flexible FFT ASIP Based on LISA 2.0," 2014 IEEE. Pp.681-687