AN IMPROVE SAR ADC USING REVERSIBLE GATES

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Abstract— **Data converters play an important role in an ever-increasing digital world which is dependent on CMOS technology. In CMOS technology, performance degradation of power is one of the foremost questions at daily vitality. The analog to digital converters ADCS are the vital branch of communication system and signal processing. Among many ADCS, successive approximation register (SAR) ADCS are suitable because of low power and small area. The objective of this project is to design the implementation of SAR block using reversible gates of ADC to optimize the power of the system. As compare to previous implementation we will reduce power to achieve better performance. In this paper, the propose 8 bit SAR ADC operates at high frequency to reduce the power in 90nm technology with Tanner tool and the reversible gates are built using buffered CMOS logic than complimentary transistors which consumes low power when compared to traditional CMOS implementation.**

***Keywords*—**: Reversible gates, successive approximation register(SAR) ADC, CMOS gate

I. INTRODUCTION

Analog to Digital conversion is an electronic process in which a continuously variable analog signal is changed without altering its essential content, in to a multilevel digital signal. In the real world most of the signals sensed and processed by humans are analog signals like light sound , conversion of audio signals (mobile, micro, digital music records,..) ,conversion of video signals like cameras ,frame, grabber etc , measurement system(speed), data acquisition system(voltage, current , temperature sensor etc) and data communication system ex. A typical modem makes use of an ADC to covert the incoming audio from a twisted-pair line in to signals the computer understand ,these are the various examples. There are different types of ADCs:

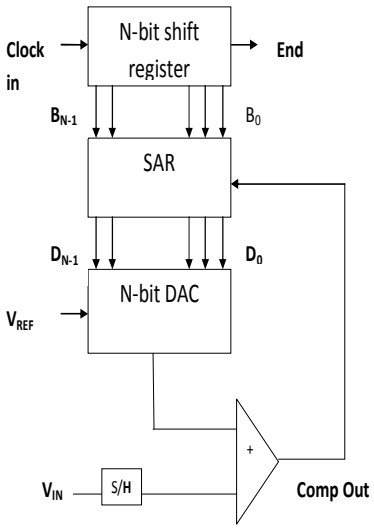
1. Direct-conversion ADC or flash ADC
2. Successive-Approximation ADC
3. Pipeline ADC

1.1 Successive Approximation ADC

A successive approximation ADC is a type of analog-to-digital converter that converts a

continuous analog waveform into a discrete digital representation and perform a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.SAR ADCS have attracted more attention because of excellent power efficiency, scalability and characteristic of digital nature .The energy limited applications such as wireless sensing devices for wearable products or portable, require high efficient ADCS for extending the battery life of these devices. SAR ADCS are also used in other applications such as high speed wireline and wireless communication systems where low power and low area require. The below diagram represents the working of SAR ADC.

Block Diagram of SAR ADC



The SAR ADC consists of N-bit shift register, SAR register, N-bit DAC, Sample and Hold circuit and Comparator.

- The input voltage V_{IN} gives to the Sample and Hold circuit to hold the value till the end of conversion.
- The output of N-bit DAC is VREF/2 which compares with input voltage.
- The output of comparator gives to the SAR register and the comparator controls the direction of binary search which perform by successive approximation converter.
- The output of SAR register is the final digital conversion..
- A successive approximation register sub-circuit designed to supply an approximate digital code of V_{IN} to the internal DAC
- Firstly, 1 is given to the B_{N-1} and all the bits remains 0, D_{N-1} is also set to 1 and all the bits remains 0.
- If the output of DAC is greater than V_{IN}, then the output of comparator is 1 and the comparator resets D_{N-1} to 0.
- If the output of DAC is less than V_{IN} then the output of comparator is 0 and D_{N-1} remains 1.D_{N-1} is the actual MSB of the digital output code.
- Again 1 is applied to the shift register is then shifted bye one position so that B_{N-2}=1, while the remaining bits are all 0.
- DN-1 is set to 1, D_{N-3} through D0 remain 0, while D_{N-1} remains the value from the MSB conversion.
- Again the output of DAC compares with input voltage.
- This process is repeated till the output of DAC converges to the value of V_{IN} within the resolution converter.

1.2 Reversible gates

The reversible logic gates have emerged as a promising technology in recent years because of having applications in low power CMOS, quantum computing, nanotechnology and optical computing. Reversible logic circuits provide less power dissipation as well as distinct output assignment for each distinct input. There is no loss of information in this gate. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional AND gate, it consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to truth table shown below,there are three inputs (1, 0), (0, 1), and (0, 0) that corresponds to an output zero. Hence it is not possible to determine a unique input that resulted in the output zero.In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output.This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an m x n function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed.

The two main constraints of reversible logic circuit is Fan out not allowed and Feedbacks or loops not allowed.

II Literature Review

1) **Kai-Hsiang Chiang . Soon-Jyh Chang, Guan-Ying huanh and Ying-zu lin**, **"A 10b100KS/s SAR ADC with Charge Recycling Switching Method."**IEEE 2014 conference.

Conclusion: This paper presents a low voltage and energy efficient 10b SAR ADC which used charge recycling switching method for saving the switching energy and a window-based reconfigurable comparator is used to achieve fast comparison and small power dissipation.Power 0.107 µ Watt.

2) **Hooman Farkhani and Mohammad Meymandi-Nejad ,Manoj Sachdev ,"A Fully Digital ADC Using A New Delay Element With Enhanced Linearity"**, IEEE 2008 conference.

Conclusion: In this paper the nonlinearity of the delay element(DE), which is the main building block in an FD-ADC, is discussed and its impact on the overall performance of the ADC is addressed. It is shown that the nonlinearity of the delay element should be within certain limits in order to achieve the best signal to noise plus distortion ratio SNDR. Also a new current starved delay element with enhanced linearity is proposed.

3) **Baiying Yu, William C . Black, Jr ,"A 900MS/s 6b Interleaved CMOS FLASH ADC",** IEEE 2001 conference.

Conclusion: This paper presents the 4 on-chip ADCs share a common reference string andpreamplifier to minimize the mismatch between channels. The time interleaved architecture increases the maximum conversion rate practical with any technology but suffers performance degradation if there is any mismatch between the channels in terms of gain, offset and timing skew. In this design all

of the ADCs within the flash array share the same reference resistor string and each comparator shares the same preamplifier stage with the other converters in the array. To a first order, this eliminates variations in reference string and comparator offset voltages from degrading performance of the converter array. Additional techniques are used to minimize interaction between converters and to minimize corruption of the input signal by regeneration induced noise. To minimize the effect of timing skew between converters, a novel clock generator is used to generate low skew four phase clocks on chip. Power dissipation 250mW.

4) **Young-Kyun Cho,Young-Deuk Jeon ,Jae-Won Nam,Jong-Kee Kwon**, **"A 9-bit 80 MS/s SAR ADC Converter With a Capacitor Reduction Technique" ,** IEEE 2010 conference**.**

Conclusion: In this paper , the 9-bit capacitor array consists of only 16 unit capacitors and a coupling capacitor due to the proposed binary weighted split-capacitor arrays with a merged capacitor switching technique. The proposed ADC includes a comparator with offset cancellation and uses digital calibration for error correction. Power is 0.2 mili Watt.

5) **Mahesh Kumar Adimulam, Sreehari Veeramachaneni,N Moorthy Muthukrishnan, M.b Srinivas**, **"A Novel, Variable Resolution Flash ADC with Sub Flash Architecture",** IEEE 2010 conference.

Conclusion: In this paper, a design for low power flash ADC with configurable resolution is proposed. A novel sub flash architecture is employed to achieve variable resolution as well as to switch the unused parallel voltage comparators and resistor based circuit to standby mode leading to the consumption of leakage power.Power 20 micro watt .

III.CONCLUSION

The main problem with the existing approach is that they do not use sophisticated MOS level techniques for power optimization. Most of the techniques used by the papers are either based on a different SAR design, or a variation in technology for implementation. But at the MOS level various different architectures are possible, and we are proposing to improve the performance of ADC using reversible gates in terms of power dissipation which will allow us achieve better working performance of the SAR ADC than existing implementations.

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