Performance Study of Heterogeneous Router for On Chip Network

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***Abstract*—Network-on-Chip (NoC) is an important communication infrastructure for System-on-Chips (SoCs). Designing high performance NoCs with minimized area overhead is becoming a major technical challenge. Router is most important parameter of the NOC. In this paper we comparing different types of routers (Heterogeneous router) i.e. The loop back virtual channel router , look - ahead speculative virtual channel and baseline router architecture . In this loopback virtual channel router, if there is a request to a busy buffer, the router will store incoming packet in any other suitable free buffer in the router. This router will be complete a look-back operation before entering a wait state. Goal of this architecture is to achieve better performance for area and latency with the help of various simulations. The architecture will be developed and simulated using hardware description language (HDL) and synthesize on the FPGA kit using Xilinx ISE.**

***Keywords*— Network on Chip (NOC), system on chips (SOC), look - ahead speculative router.**

I. INTRODUCTION

Network on chip form only efficient and scalable solution to provide global on chip communication in large VLSI design. In semiconductor technology recent trends suggest use of packet switched based networks as the intercommunication in system on chip design generally poor routing design (i.e. heavy buffer) results in the movement of packets across on on-optimal paths that packets. Not reaching destination and increase power consumption, inversely in good routing data flow accurately and reduces latency.

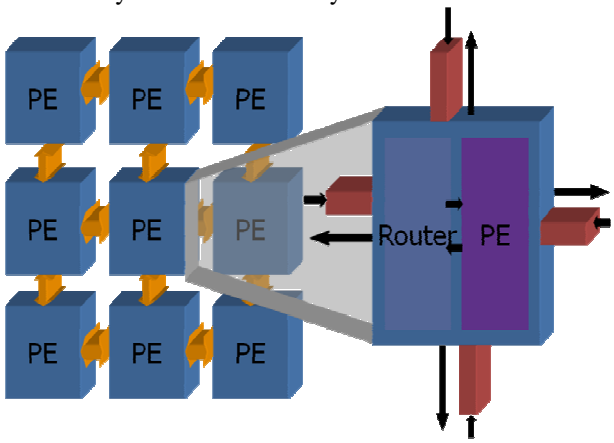

Figure - 1. Network On Chip Architecture

Network congestion and packet delay as well as starvation, deadlock all this problem are reduced significantly in virtual channel router. Each router consist of the following components : 1) A link controller, which is an adapter / interface between the topology and the actual logic routing; 2) Input /Output buffer which are local storage elements for efficient routing ; 3) An arbiter, allowing arbitration logic implementation for efficient routing; and 4) Physical crossbar switch or switches[1].

Network on chip architecture router can handle many operation like large number of buffer, high throughput and to avoid potential deadlock or starvations during transferring of data from one place to another. At each input, port buffers are organized as separate or multiplexed FIFO queues, creating an array of either physical input buffers or virtual channel buffer. This is done to accommodate high throughput packet flow to the output ports. [1] In virtual channel input buffer and VC allocator both allocate the incoming packets to virtual channels.

Look-ahead routings is another technique that removes the serialization delay due to routing computation by determining the route of a packet one hop in advance [6], [7], [8]. we have implemented the proposed router on FPGA and evaluated in terms of communication latency, through put and hardware amount [3]. The simulations are carried out by one 4x4 two-dimensional mesh network developed in VHDL besides, the VC router with baseline and look-ahead speculative architectures are also implemented for comparison.

Outline for this paper is as follows: After the introduction we discussed the overview of look-ahead speculative and base line router architecture as well as literature review In section II. Further we introduce switching technique and packet structure in section III. As well as in section IV proposed look-back virtual channel router architecture in details. The different blocks of simulation result are carried out in section V. And finally we draw a conclusion in the last section.

II. BACKGROUND

In this paper we are studying baseline router , look-ahead speculative router and loopback virtual channel router. We should first explain the base router architecture and its operation. As illustrated in figure 2. The basic router consist of five input port and five output port connected together using

the intermediate crossbar. In mesh topology, each input and output port is associated with a specific direction: East, West, North, South and local. The local input and output ports are connected to the network interface which is connected to the processing element[3].

The input port receives the incoming data packet form each direction and stores them in FIFO buffer. The routing algorithm determine the packet route according the destination address within the packet header. In order to select appropriate output port, a crossbar switch is design to have a communication link between requesting input and its destined output port.

In output port arbiter is required to determine how to resource is shared amongst many requesters. When putting and arbiter into a design many factor must be considered. Interface between the requester and the arbiter must be appropriate for the size and speed of the arbiter [2] If many flits arrive at buffers from several virtual channels as these flits are destined for one physical channel, arbiter receives request signals from buffer such as FIFO empty for full signals. These FIFO empty and full signal are generated by comparing write pointer and read pointers. Output controller handle the communication with downstream router. MUX selects which packet goes to the downstream router according to the arbiter selection [3]

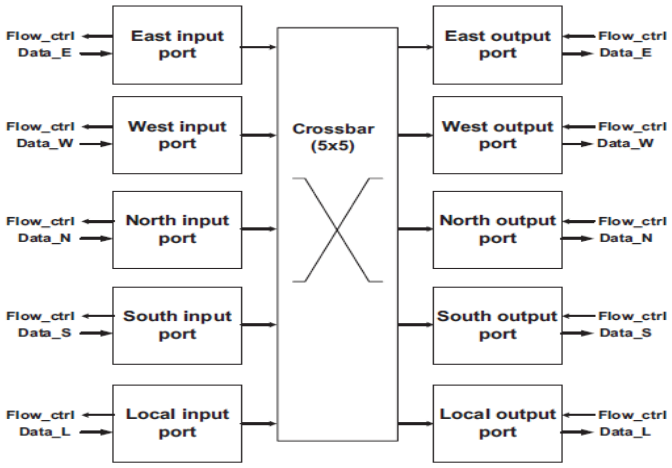

Figure - 2. Basic router architecture

Figure-2 shows the architecture of a conventional baseline VC router [4] that is referred as the basis in our work. The major components of the router include the input buffers, routing computation logic, VC allocator, switch allocator and crossbar switch. In this model, a packet is generally divided into multiple flits (flow control digits) where the head flit contains all the necessary routing information and the following flits carry payload data. A head flit will advance to the output channel through four pipeline stages that consist of the routing computation (RC), VC allocation (VA) for determining the output channels, switch allocation (SA) for allocating the time slot on the crossbar switch and output channels, and switch traversal (ST) for transferring flits through the crossbar. Once the head flit completes the computation of a route and allocation of a VC, there is nothing to do for remaining flits in the RC and VA stages. However, they cannot bypass these stage and advance directly to the SA stage because they must remain in order and behind the head flit. If each of the pipeline stage is performed in one clock cycle, at least four clock cycles are required to transfer a head flit through a router. Obviously, this delay at each router causes progressive latency on the interconnection networks. As shown in Fig. 1, it consists of five input ports and five output ports, connected together using the intermediate crossbar. In a mesh topology, each input and output port is associated with a specific direction: East (E), West (W), North (N), South (S), and Local (L). The local input and output ports are connected to the network interface which is connected to the processing element (PE). The structure and the functionality of the input and output ports is explained as follows:

1) Input port: Any input port consists of three main components (Fig. 2):

a) Input controller: It is responsible for receiving the requests (req_UP) from the upstream router and giving the grants (gnt_US) if the FIFO is not full. Also it sends the internal requests (req_int) to the output ports and waits for their grants (gnt_int) in order to transfer the received packets to their downstream routers according to the routing logic used.

b) FIFO buffer: To store the incoming packets (pkt_US) from the upstream router.

c) Routing logic: Applies the routing algorithm to the header packet of the FIFO to determine the packet direction according to the destination address within the packet in order to choose the apropriate output port.

2) Output port: As shown in Fig. 3, it also consists of three main components:

a) Arbiter: Receives all incoming requests (req_int_E,W, N,S,L) for the output port and then grant one of them (gnt_int_E,W,N,S,L) according to a prespecified logic. There are many arbitration logic functions stated in [8], we chose Round Robin because of its simplicity and fairness.

b) Output controller: Handles the communication with the downstream router (using req_DS and gnt_DS signals).

c) MUX: Selects which packet goes to the downstream router according to the arbiter selection.[3]

The main limitation during the Base router operation is the contention problem. Contention occurs when a request at some input port is blocked because the requested FIFO of this port is full. Such contention may lead to other blockings in the network and hence congestion occurs [8], which degrade the performance of the overall network.

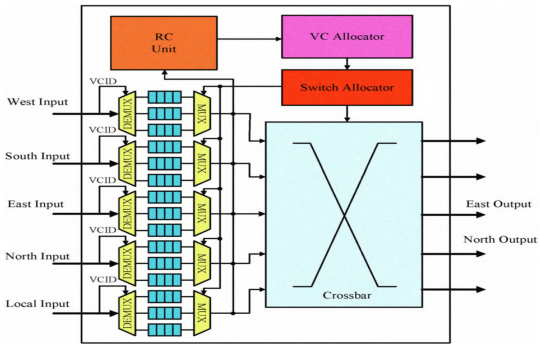

Figure - 3. Architecture of baseline router

The look-ahead routing is another technique that reduces the number of pipeline stages by performing the routing computation ahead of time to remove it from the critical path [6],[7],[8]. In this mechanism, each router performs the routing computation for the next hop (denoted as NRC) and pass the result along with the head flit. Employing this type of one-hop route look-ahead shortens the four stage pipeline to three-stage. Since the control dependency between the routing computation and others is removed, the NRC and VSA can be performed in parallel to attain two-stage pipeline. However, performing numerous pipeline stages in parallel may lead to the degradation of frequency and the need of complex control logic.

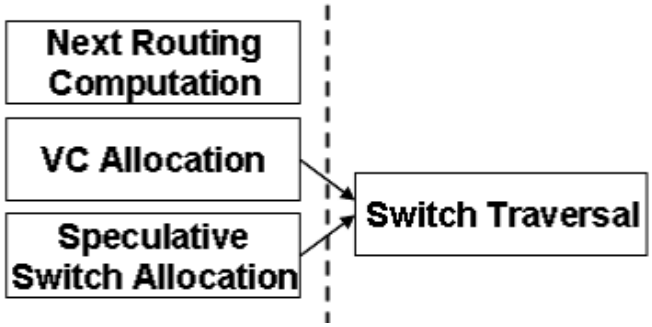

Figure- 4. The look-ahead speculative routing

Heterogeneous router like as baseline router ,look- ahead speculative router and loopback virtual channel router are compared with each other. More latency and contention problem occurred in baseline router compared with look-ahead speculative router. In look-ahead speculative router has less latency but it heavily loaded then it becomes in efficient.Further comparative evaluation work of loopback virtual channel router is in process.

This paper [1] proposes a loopback input buffer virtual channel (LB-VC) buffering structure and mechanism to a)reduce latency of the packet/flit in the router, b)avoid HEAD-OF-Line (HOL) blocking of packets/flits, and c) reduce buffer overheads in the NOC router. Compared to classical router micro-architecture, this architecture achieves better performance for area, latency and power. This paper [2] the speculative virtual channel router for network on chip (NOC)and non-speculative virtual channel router for network on chip (NOC). In speculative virtual channel router, speculative virtual channel allocation and speculative switch allocation takes place at the same time on the other hand in non speculative virtual channel route channel allocation and switch allocation takes place serially. In this paper [3] we introduced a new flexible router architecture that can improve the performance of the overall network using the same amount of buffering available but in an efficient way. This paper [4]can be proposed on the fly virtual channel (VC) allocation for low cost high performance on chip router. By performing the VC allocations base on the result of switch allocation, dependency between VC allocation and switch traversal is removed and these stages can be performed in parallel. This paper [5] is to provide a guideline to optimize virtual channel router architecture for NOC. If you are to evaluate network performance of virtual channel router with different number of virtual channel , buffer depths, and find out efficient buffer scheme for the virtual channel router. According to the simulation results, network performance is improved when the number of virtual channel increases. But too many virtual channels are not efficient for mesh base NOC.

III. SWITCHING TECHNIQUE AND PACKET STRUCTURE

Switching techniques have a huge impact on the design of router architecture and broadly classified as circuit switching and packet switching. Circuit switching is a methodology of implementing a telecommunication network in which to network nodes establish a dedicated communication channel through the network before the node make communicate. Now a days packet switching is most effective technique are used in current NOC design. Packet switching transfer data by segmenting longer massages into smaller data packets and forwarding these packets individually from the sender to the receiver possibly with different routers and delay for each packet. There are three basic types of packet switching schemes. Store and Forward (SAF), wormhole (WH) and Virtual Cut Through (VCT) switching SAF first stores the incoming packets into the input buffer. The router in every hop must wait to receive the entire packet before forwarding header flit to the neighboring router. Main advantages of the routing is they support elaborate routing algorithms [1].

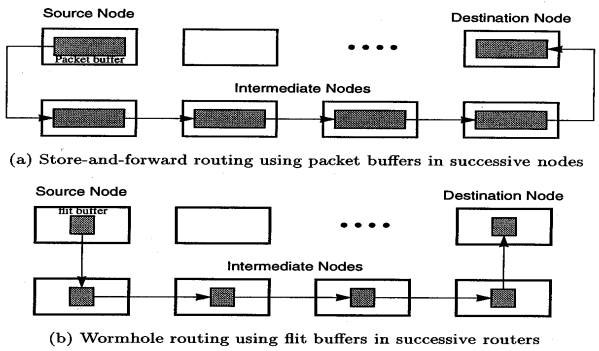

Figure- 5. Switching Technique

Virtual Cut Through (VCT) switching does not wait for a packet to be received completely before making routing decision [10]. It can forward the header flit before the next flit of packet arrives. It has advantages of low latency and less HOL blocking. In WH routing a packet is divided into a number of flits for transmission WH routing operates by advancing the head of a packet directly form incoming to outgoing channels of the router [7]

A packet consist of three types of flits : head flit, body flit and tail flit. A head flit contains control data such as routing information of the packet, the body flit contains transferring data and the tail flit indicate the end of the packet. A packet is divided into multiple flits where a the head flit contains all the necessary routing information and the other contains data elements. Is split is formed of three fields : TYPE for the type of flit, VCID for the VC identification and DATA for the data payload the head flit is special case

IV. LOOPBACK VIRUTAL CHANNEL ROUTER ARCHITURE

A novel input buffer (IPB)/VC buffer structure and switching architecture is proposed that minimizes the router buffer overhead, avoids HoL blocking, and minimizes packet/flit latency[]. The top-level router micro-architecture of the proposed loopback IPB/VC (LB-VC) is shown in Figure 6.

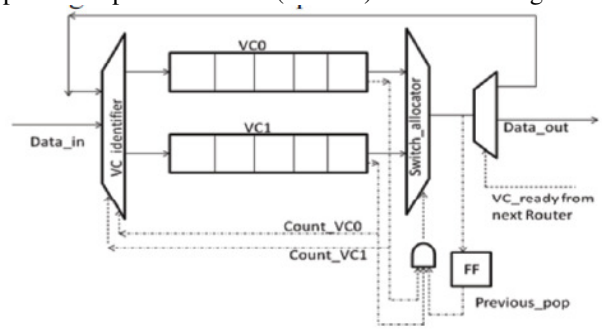

Figure -6 .Proposed loopback virtual channel Router Architecture

The loopback virtual channel router micro architecture consist of the following components: 1) VC identifier 2) VC FIFO buffer and 3) A switching allocator (SA) which implements the buffer selection logic. Virtual channel controller (VC). In virtual channel buffer contains packet information on a flit level, flits traversing a router flow through virtual channels. These are implemented by dedicating one virtual channel buffer (VCB) to a connection This unit is responsible for multiplexing the contains of the virtual channel on to the physical links. Several efficient arbitration scheme have been proposed.

If more then one connection require the simultaneous use of a specific link, the flits need to be arbitrated from their VCBs onto the link. The most common approach is simple round-robin [14] arbitration among the VCBs. Virtual channels are then granted slots based on their bandwidth requirements, in effect performing a weighted time-division-multiplexing (TDM).[9] The packet is loopback that is, packet is sending back and push back into VC based on the VC utilization. If all output port are congested then VC is completely utilize and Predecessor router is inform of the congestion of the router. The SA perform one complete loopback operation before entering a wait state [1]. The change in output router control signals trigger the execution of the SA operation .

The proposed loopback virtual channel router architecture uses the mesh and WK-recursive topology, SAF and WH switching techniques, and the XY routing algorithm. The NOC system that will be implemented consist of five main modules: 1) the processing architecture, 2) the communication infrastructure, 3) the Communication paradigm 4) the monitor module and 5) the traffic generator module [1]. The processing architecture module consisted of a processing element (PE) and a network adapter module.

In FIFO buffer and flow control the queue acts as a FIFO buffer and is implemented as a large signal 1-read 1-write register file. The queue is seventy six bits wide and sixty four flits deep. There are four separate queues per physical port to support virtual channel read and write to different location in the queue occur simultaneously in a single clock cycle. This approach helps to reduce overall bit line loading.

In summary the advantage of micro architecture include the reduction of packet, latency, reduction of VC area overhead and mitigation of HOL blocking and better performance than other comparative router. In order to evaluate the purposed micro architecture a NOC frame work will be implemented in VHDL. Hardware description language (HDL).

V. SIMULATION RESULT

The different blocks of the router are designed with the help of VHDL coding and simulation results are obtained through test bench. The figure 6 to 9 indicates the functional verification of the different blocks. The simulation of input port router shows that the input data flit is transferred to the respective virtual channel and is available at the output after a clock cycle delay.

Crossbar switch is the soul of data routing. crossbar switch is used for routing data from one input port to many output port. Simulation of crossbar results in transfer to input to output as per the arbitration scheme shown in the simulation results of arbiter. Arbiter is integral part of crossbar switch which makes crossbar a contention free. Functional simulation of loop back router depicts transfer of packets from input to output.

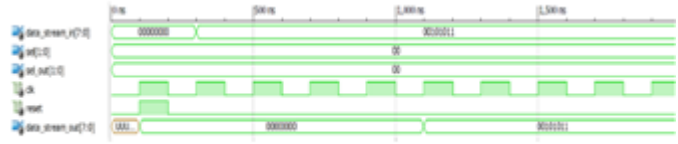

Figure 7: Simulation Result of Input port

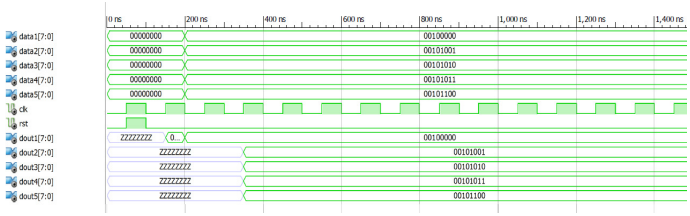

Figure 8: Simulation Result of Cross bar

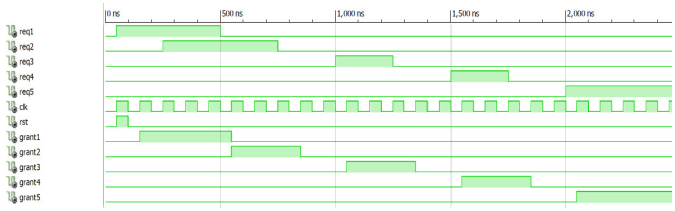

Figure 9: Simulation Result of Arbiter

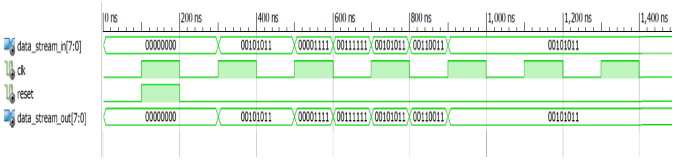

Figure 10: Simulation Result of loopback router

VI. CONCLUSION

The simulation results of different blocks of the router in previous section verify the design of the router. The design is implemented in Xilinx ISE 13.1 on device XC3S200 that shows that the router with virtual loop-back router occupies less area than baseline router. This paper compares baseline router and look ahead router. Comparisons result shows that baseline router has contention problem which degrade the performance of the overall network . And look-ahead router degrade the frequency. This drawback is reduce in loopback virtual channel Router. The future scope of the work is to connect this design to matlab to analysis the performance by injecting packets into router and calculating the delay and throughput.

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