A REVIEW PAPER ON DESIGN OF FPGA BASED HIGH SPEED NOTCH FILTER USING PARALLEL PROCESSING

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***Abstract*— In this, we present a Field Programmable Gate Array (FPGA) based design and implementation of extremely high speed tunable IIR Notch filter. Here we will propose FPGA based Notch filter whose frequency is 1.2Gsps with the help of parallel processing. For speed up factor new and easy method of Pascal's Triangle is used to calculate multiplier coefficient for feed forward and feed backward section of extremely high speed Notch filter**

***Keywords*—**: Scattered Look Ahead Parallel process, Pascal Triangle, Tunable Notch filters, unfolding.

I.INTRODUCTION-:

The Notch filter is used to Notch out particular frequency from input signal. The requirement of digital Notch filters to operate at extremely high clock frequency in the order of (Giga samples per second Gsps). We propose FPGA implementation of extremely high Speed Notch filter applying standard technique of parallel processing.

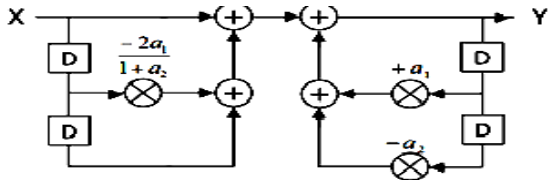


FIG1]. 2nd ORDER IIR NOTCH FILTER STRUCTURE

DERIVE MULTIPLIER COEFFICINT USING PASCAL'S TRIANGLE METHOD:

The coefficient of transfer function can be calculated by using this easy and new method. The values of coefficient can be calculated by subtracting values of square from circle. The first coefficient value is 16-0=1, The second coefficient value is 105-1= 104, The third coefficient value is 364-12=352. In this way coefficient of transfer function of filter is obtained.

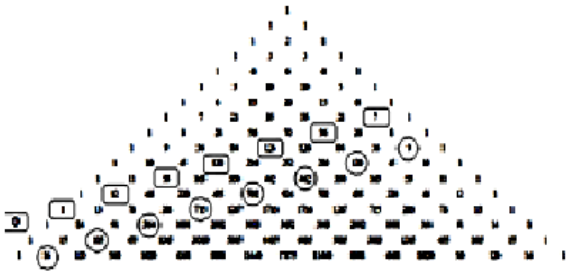


FIG2]. PASCAL'S TRIANGLE TO DERIVE MULTIPLIER COEFFICIENT

A FPGA BASED DESIGN OF EXTREMELY HIGH SPEED NOTCH [Parallel processing of IIR Notch filter]

To introduce 16 or multiple of 16 for parallel processing in the feedback loop the basic IIR Notch filter is decomposed with SLA16 as show in fig below. The 4- unfolded version of IIR Notch filter is as shown. It contains 6 stages, the Forward Stage and 1 Feed Backward

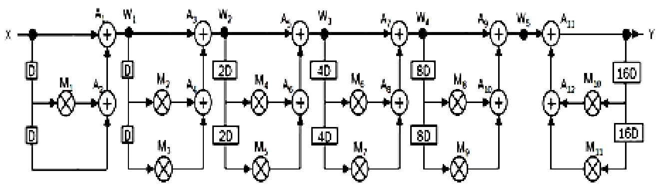
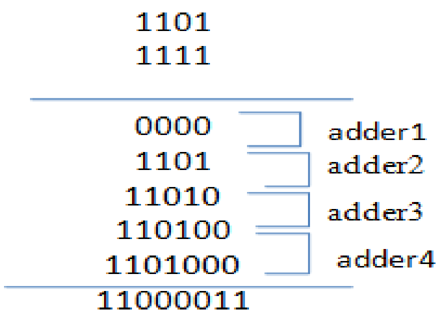


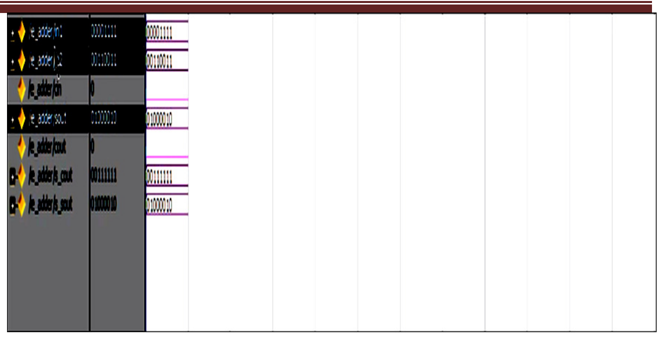
FIG3]. FULLY PIPELINED WITH SLA 16 DECOMPOSED IIR NOTCH FILTER

To create Notch filter we required ADDER and Multiplier. Consider multiplication of two four bit number .



WAVEFORM-:

A] SIMULATION FOR ADDER



B] SIMULATION FOR MULTIPLIER

CONCLUSION-:
FPGA based design and implementation Methodology of extremely high speed tunable notch filter is presented. The concept of pipelining, retiming, unfolding and high-speed. A new efficient and easy technique has been used to calculate the multiplier coefficients of extremely high speed IIR notch filter using PASCAL triangle.

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