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Design And Analyze Power Efficient BCD Adder Using Different Digital Logic Techniques

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Abstract— This paper proposed the design of high speed BCD adder using digital logic technique. An adder is a digital circuit that performs addition of numbers. The adder is one of the most critical components of a processor. Adders are used not only in the arithmetic logic unit (ALU), but also in other parts of the processor. The BCD adder is designed using transmission gate (TG), Multiple Threshold CMOS (MTCMOS) and Gate Diffusion Input (GDI) technique on Tanner SPICE simulation. Performance evaluation of design using recent logic techniques and their respective obtained parameter will give most efficient technique to implement BCD adder for respective parameter.

Keyword- Full Adder, 4 Bit Binary Adder, BCD Adder, MTCMOS, TG, GDI.

I.INTRODUCTION:

The adder is one of the most critical components of a processor; Adder is used in the Arithmetic Logic Unit (ALU) and in the other part of processor. And its increasing demand for mobile electronic devices such as cellular phones and laptop computers. It is requires the use of power efficient VLSI circuits.

Full adder is the fundamental unit in circuits used for performing arithmetic operations i.e. addition, multipliers and comparators. Therefore, It reducing power consumption of the BCD adders, It will reduce the overall power consumption of the whole system. The arithmetic operations are used as digital signal processing, image processing and microprocessors of the VLSI application.

Transmission Gate:

Transmission gate is act as a simple switch circuit. Switch circuit is present a new class of logic circuits that used pass transistors or TG. The CMOS transmission gate consists of one PMOS and one NMOS transistor, connected in parallel. The gate voltages applied to these two transistors as complementary signals. The CMOS TG operates as a bidirectional switch. The bidirectional switch is between the nodes A and node B which is controlled by signal C. If the control signal C is equal to VDD, and then both transistors are turned on and It provide a low-resistance current path between the nodes A and B. If, on the other hand, the control signal C is low, and then both transistors will be off, and the path between the A and B will be an open circuit. Fig. I. also shows three other commonly used symbolic representations of the TG.

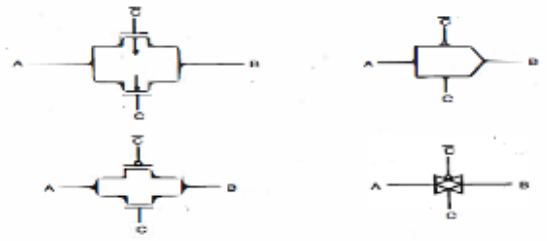


Fig I-Symbolic representations of the transmission gate

MTCMOS Technique:

Supply and threshold voltages are reduced with the scaling of CMOS technologies. The threshold voltage leads to an exponential increase in the subthreshold leakage current. In modern high performance integrated circuits (ICs), more than 40% of the total active mode energy can be dissipated due to the leakage currents. Leakage currents will soon dominate the total energy consumption of high performance ICs. A popular low leakage circuit technique is the Multithreshold Voltage CMOS (MTCMOS).

The multi threshold CMOS technology has two main features. First, “active” and “sleep”

operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as "power gating". The schematic digram of power gating technique using MTCMOS is shown in Fig. II. The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate the low threshold voltage.

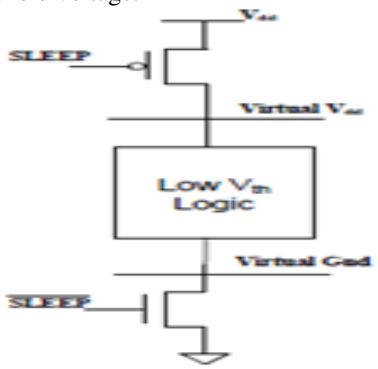


Fig. II. Power Gating Technique using MTCMOS.

transistors from supply voltage and ground during standby (sleep) mode to prevent leakage dissipation.

In the active mode, sleep transistors are turned on and the logic consisting of low *VT* transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high *VT* transistors are turned off causing isolation of low *VT* transistor from supply voltage and ground thereby reducing sub-threshold leakage current.

GDI Technique:

BASIC GATE DIFFUSION INPUT (GDI CELL) FUNCTIONS

Gate Diffusion Input (GDI CELL) method is based on the use of a simple cell as shown in Figure - 1. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: (1) Gate Diffusion Input (GDI CELL) contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS technologies. A simple change of the input configuration of the simple Gate Diffusion Input (GDI) CELL as shown in figure III corresponds to six different Boolean functions.

1. When input N=0, P=B, and G=A then output D= *AB* which is function F1.
2. When input N=B, P=1, and G=A then output D= $\overline{A}$+*B* which is function F2.
3. When input N=B, P=0, and G=A then output D=AB which is AND function
4. When input N=1, P=B, and G=A then output D=A+B which is OR function.
5. When input N=C, P=B, and G=A then output $\overline{D}$= *AB* +*AC* which is MUX function.
6. When input N=0, P=1, and G=A then output D= *A* which is NOT function.

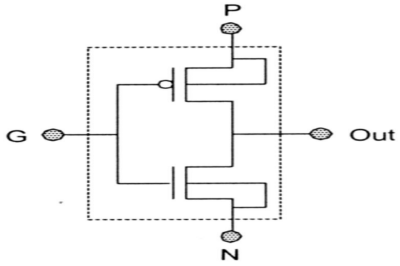


Fig -III: Gate Diffusion INPUT (GDI) Basic Cell

TABLE also shows a simple change of the input configuration of the simple Gate Diffusion Input (GDI) CELL corresponds to six different Boolean functions. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard CMOS implementations, but very simple (only 2 transistors per function) in Gate Diffusion Input (GDI CELL) design method. Gate Diffusion Input (GDI CELL) structure is different from the existing CMOS techniques and has some important features, which allows improvements in design complexity level.

N	P	G	D	Function
0	B	A	$\overline{A}$	F1
B	1	A	$\overline{A}$ +B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}$B+AC	MUX
0	1	A	$\overline{A}$	NOT

III. IMPLEMENTATION

BASIC FULL ADDER

A full adder circuit is one of the basic building blocks of the digital design. The full adder

operation can be stated as follows: Given the three 1-bit inputs A, B, and Cin, it is to calculate Sum and Carry i.e.

$$Sum = (A \text{ xor } B) \text{ xor } Cin$$

$$Carry = A \text{ and } B + Cin (A \text{ xor } B)$$

TABLE II. TRUTH TABLE OF FULL ADDER

INPUT			OUTPUT	
CIN	A	B	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1. FULL ADDER BASCED ON TRANSMISSION GATE

The 20 transistors full adder has 20 numbers of transistors to perform the full adder function. The structure is given in the fig III.

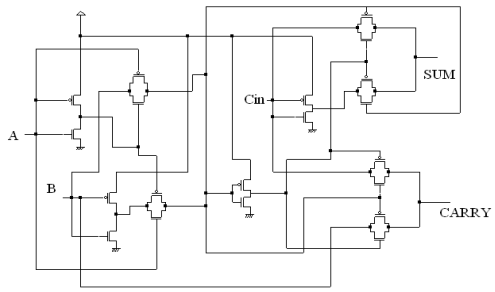
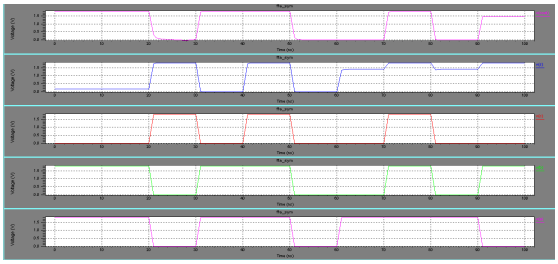


Fig III. Structure of Full Adder using TG.

Waveform of full Adder using transmission gate Fig IV.



2. FULL ADDER BASCED ON MULTIPLE THROSHOLD CMOS LOGIC:

Fig V. shows the circuit diagram of a one-bit full adder using the proposed technique in SOI CMOS technology

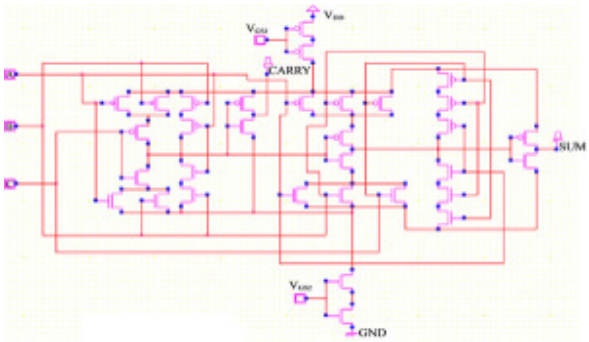
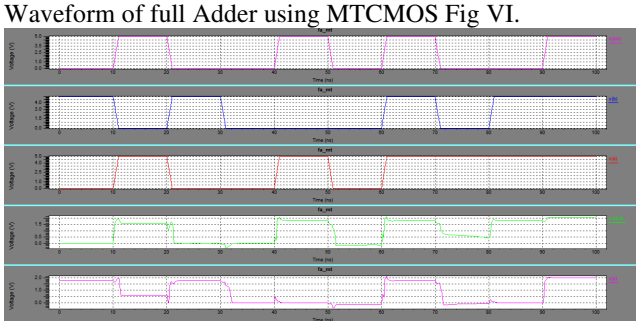


Fig V. Structure of full adder using MTCMOS.

Waveform of full Adder using MTCMOS Fig VI.



3. FULL ADDER BASCED ON GATE DIFFUSION INPUT:

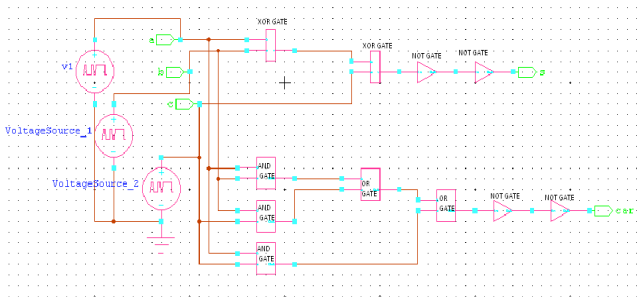
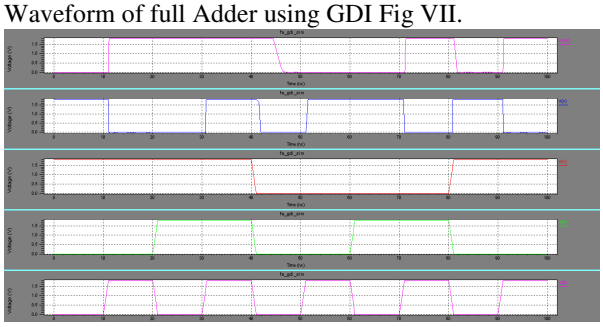


Fig VI. Structure of full adder using GDI.

Waveform of full Adder using GDI Fig VII.



4. 4 BIT BINARY ADDER USING FULL ADDER

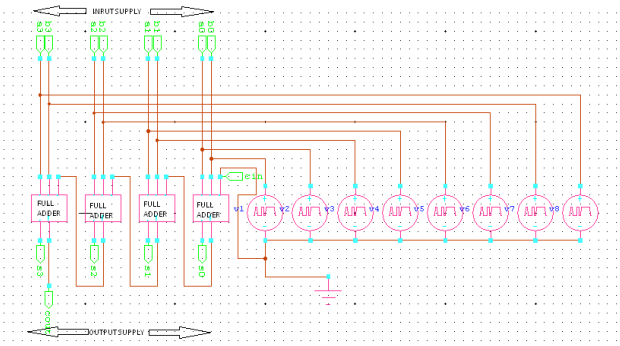
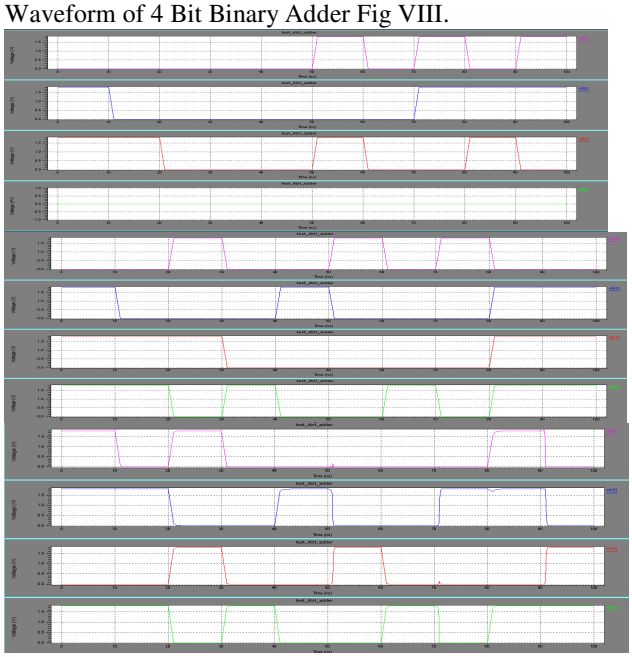
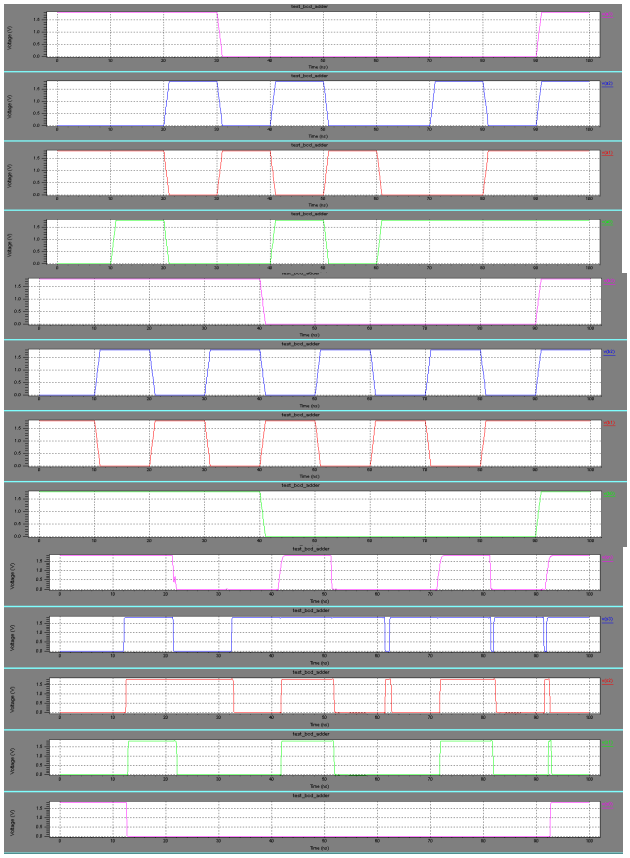


Fig VII. Structure of 4 Bit Binary Adder.

Waveform of 4 Bit Binary Adder Fig VIII.





4. BCD ADDER USING 4 BIT BINARY ADDER

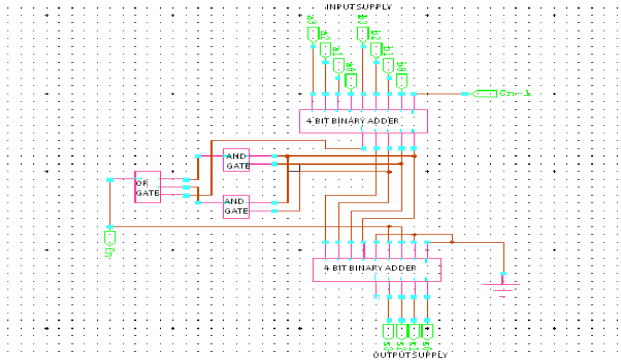


Fig IX. Structure of BCD Adder

Waveform of BCD Adder Fig X.

IV.COMPARISON AND RESULT:

Table II. shows a comparative study of the performance parameter of the proposed BCD adder employing Transmission gate(TG) with respect to a BCD adder employing multiply threshold CMOS (MTCMOS) and Gate Diffusion Input (GDI).

TABLE III.COMPERTIVE STUDY OF THE PERFORMANCE PARAMETER OF BCD ADDER

	Full Adder			4 Bit Binary Adder			BCD Adder		
	No. of Transistor	Power Dissipation (Watt)	Delay (ns)	No. of Transistor	Power Dissipation (Watt)	Delay (ns)	No. of Transistor	Power Dissipation (Watt)	Delay (ns)
TG	20	2.2046 X 10x-4	0.085	80	4.1239 X 10x-6	0.335	180	2.6382 X 10x-8	0.095
MTCMOS	28	1.5355 X 10x-5	0.16	112	1.5763 X 10x-6	0.085	236	1.9521 X 10x-6	0.08
GDI	26	1.7235 X 10-6	0.17	104	9.7982 X 10x-8	0.08	220	5.5569 X 10-6	0.165

V. CONCULSION:

It has been observed that TG is most effective in terms of transistor count as it requires less no of transistors, delay and least power consumption in GDI. The advantage of GDI technique is two transistor implementation for logic function. This together with positive measurement and simulation results, provide evidence that the GDI design might enrich the toolbox of VLSI designers.

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