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# DESIGN AND SIMULATION OF REVERSIBLE VEDIC DIVIDER

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**Abstract**

Everyday new technology is being developed which is fast, compact but more complex than its predecessors. The increase in frequency of clock to achieve greater speed of the system and increase in number of transistors which are embedded into a chip to achieve complexity of a conventional system results in increased power consumption. Almost all the gates used in the chip to perform logical operations in a conventional computer are irreversible. Reversible logic is gaining interest in the recent past due to less heat dissipating characteristics. It is proved that any Boolean function can be implemented using reversible gates. Every time a logical operation is performed some information about the input is erased or lost is dissipated as heat. Reversible logic circuits are increasingly used in power minimization. The hardware computation using regular that is irreversible gates results in power dissipation due to information loss. The methods of Vedic math has been the source of inspiration for many centuries in the field of computation. In the current binary world of high speed processing, it is necessary to have time and space efficient methods for performing arithmetic operations. Hence, in the proposed system we have designed reversible divider to reduce power dissipation while performing division.

Key words : Reversible Logic, FPGA, VHDL, Vedic

**Introduction**

In any design of Digital signal processing or microcontrollers arithmetic and logical operations are the main components. Divider circuit includes subtractor and shift registers. The basic important requirement of a Digital Signal Processing system is high speed, low power and small area. To put these considerations in the designing of a divider reversible logic gates are used. The reversible logic gates reduces power dissipation of the circuit. The divider is designed using Reversible logic gates in order to minimize the power dissipation. The reversible logic gates helps in Quantum Cost Approach. The speed of the processor can be improved by reducing the number of divisions performed per unit time. Hence the system performance and efficiency increases.

Reversible gates are circuits that have one to one mapping between inputs and outputs. Thus, the vector of input states can be always reconstructed from the vector of the output states. Design which does not result in information loss is called reversible. It takes care of the heat generated due to information loss. Bennett proved that zero energy dissipation would be possible only if the network consists of reversible logic gates. Thus, reversibility will become an essential part in future circuit design technologies. The outputs can be obtained from the inputs and inputs can be reconstructed from outputs. This is one of the differences of reversible logic gates compared to normal logic gates. So that there will be less energy loss present in the circuit.

**Reversible Gates**

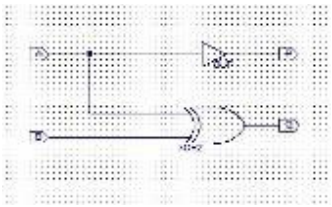
Reversible logic is a promising design which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. The fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system. The probability of a quantum particle occupying a particular state at any given time and the quantum electrodynamics between electrons when they are in that proximity. The basic principle of reversible computing is that it has an identical number of input and output lines that will produce a computing environment where the electrodynamics of the system allows for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those which do not contribute to the reversible logic realization of the design. Quantum cast refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions.

The following are the important design constraints for reversible logic circuits.
1. The gates do not allow fan-outs.
2. These circuits should have minimum quantum cost.
3. To produce minimum number of garbage outputs the design can be optimized.
4. The circuits must use minimum number of constant inputs.
5. The circuits must use a minimum gate levels.

The basic reversible logic gates used during the design are listed below:

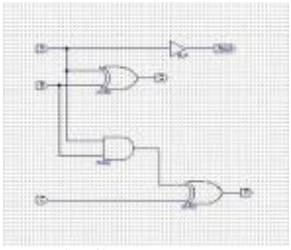
**Feynman Gate:**

It is a 2x2 gate and its logic circuit is as shown in the figure. It has quantum cost 1 and is generally used for Fan Out purposes.



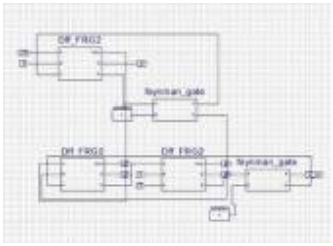
**Peres Gate:**

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost 4. It is used to realize various Boolean functions such as AND, XOR.



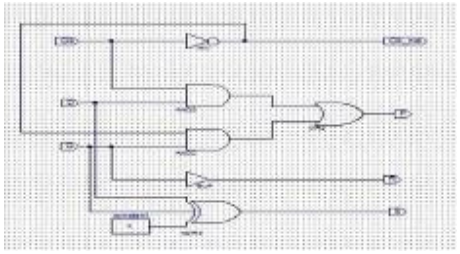
**Fred kin Gate:**

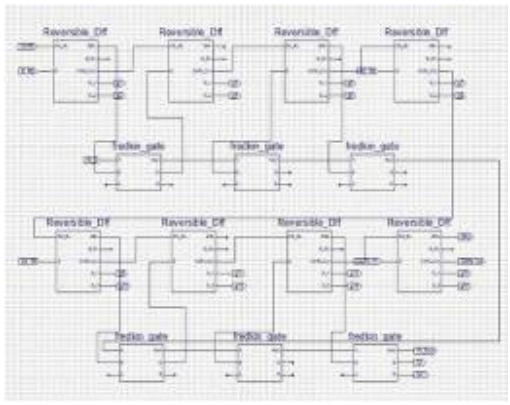
It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost 5. It can be used to implement a Multiplexer.



**AS Gate**

The reversible A S gate i s a 4 x4 r eversible g ate w ith inputs(A,B,C,D) and with outputs A', AB + A'C, D (AB + A'C) and B C.



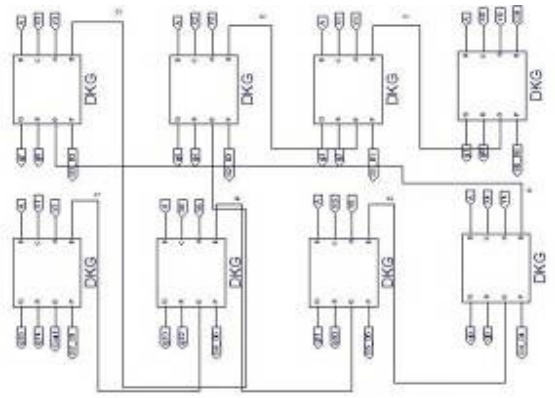


**Reversible Shift Register:**

A shift register is a cascade of flip flop, shares the same clock in which the output of flip flop is connected to the data input of the next flip-flop in
the chain, resulting in a circuit that shifts by one position t he " bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. Generally, shift register can have both parallel and serial inputs and outputs. These are often configured as serial-in, parallel-out (SIPO) or as parallel-in, serial-out (PISO). There are also types that have both serial and parallel input and types with serial and parallel output.

**Reversible Adder / Subtractor**

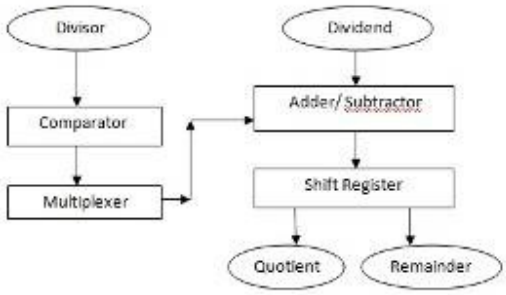
The approach of the design followed here focuses on the reversible full adder and subtractor together in a single unit. This logic of the design is implemented using VHDL code and simulated using Isim simulator. The functionality of the individual gates is implemented using Behavioral and the structural style of modeling.



**Proposed Plan**

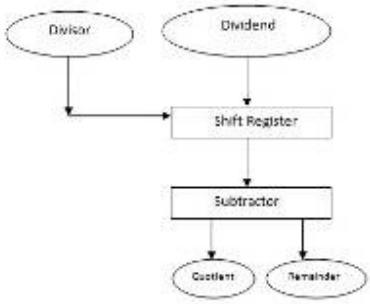
In the proposed plan, the design of divider is designed on the logics of Vedic mathematics. This design uses less power and highly efficient. In the conventional divider circuit power consumption is more. In this paper, the vedic method which is used shows power consumption of a divider circuitry were minimized significantly by removing unnecessary recursion through conventional vedic division methodology. The hardware required in the circuit reduces which improves the speed of the divisor. In the conventional method, a divider circuit uses adder, subtractor, and shift register, multiplexer, complementing and comparator circuit.

**Fig**. Design of Conventional Divider




In the proposed system the design has subtractor and shift register, therefore reducing the hardware.

**Fig**. Design of Reversible Divider circuit using Vedic Method




**Vedic Division**

After analyzing the division algorithms from Vedic math, Kennedi has tried to develop a fast and efficient division method. This method is to be compared with current Booths algorithm through spectacles of Vedic math. In conventional method if we divide the number repeatedly by two and shifting to right by one bit position we increase the iteration and hence the required for reaching closer to the result. This also requires memory read/write cycles and power.

All these issues are reduced in proposed algorithm by block

| | | | |
|---|---|---|---|
| (A) | Shifted by how many positions -value | 4 | 16 |
| (B) | Shifted by how many positions -value | 2 | 4 |
| (C) | Shifted by how many positions -value | 1 | 2 |
| (D) | Shifted by how many positions -value | 1 | 2 |
| (E) | Shifted by how many positions -value | 0 | 1 |
| (F) | Quotient | | 25 |

shifting divisor to one position. The shift counter is stored in memory. Hence, we add all memory locations to get quotient and remainder.

The method works as follows.
The proposed algorithm is suitable for any size of numerator and denominator. As result is accumulated in one place, very less memory is required and the consumption of power is less.

The Divider Circuit

In this proposed system the division of any number of bits can be done. After analyzing different Vedic methods, it was found that the processes involved are involved in getting the results. The proposed algorithm requires least number of processes. Hence this method will be very

economical, efficient and the consumption of power will be reduced.

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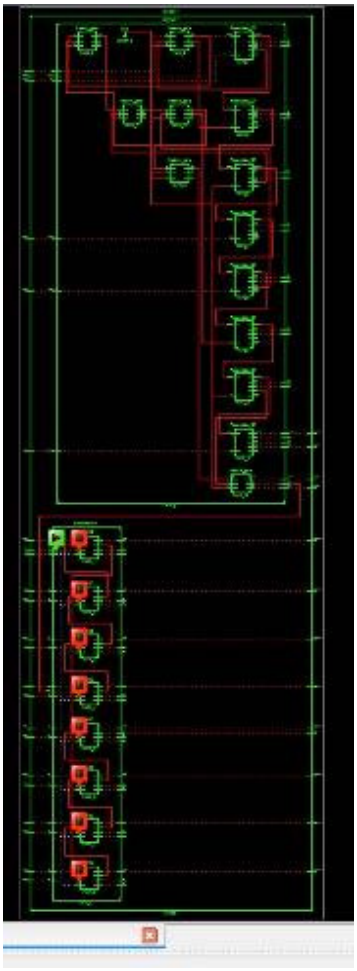
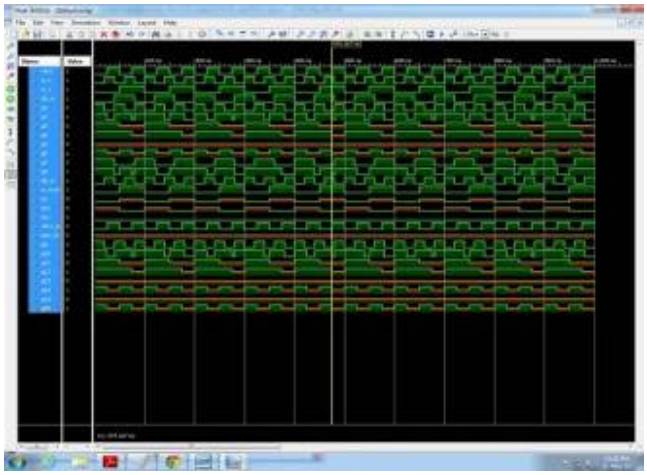
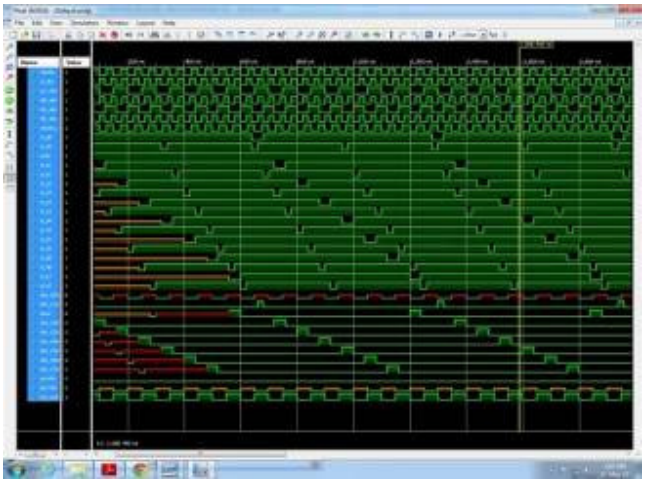




**Simulation of Reversible Vedic Divider Circuit**



**Simulation of Reversible Divider Circuit**

**Conclusion**

After analyzing different Vedic methods, it was found that the processes involved are involved in getting the results. The proposed algorithm requires least number of processes. Hence this method will be very economical, efficient and the consumption of power will be reduced.

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