DESIGN OF HIGH-SPEED HYBRID CARRY SELECT ADDERS USING VHDL

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***Abstract*— Carry select adder (CSA) is a square-root time high-speed adder. CSA is one of the fastest adders used in many data processing systems to perform fast arithmetic operations. In this project we propose to design hybrid carry select adders with a focus on high speed. CSA is a compromise between the longer delay Ripple carry adder (RCA) and the shorter delay Carry look-ahead adder (CLA). Conventionally carry select adders are realize using the full adders and 2:1 multiplexers. On the other hand hybrid carry select adders involve a combination of carry select and carry look-ahead adders.In this work, we propose to design hybrid carry select adders involving carry select and carry look-ahead adders with and without ripple carry adder (RCA) using very high speed integrated circuits hardware description language (VHDL).**

***Keywords*—** *Carry select adder, Ripple carry adder, Carry look-ahead adder, VHDL code*

I. INTRODUCTION

Carry select adder (CSA) belongs to the family of high speed square-root time adders and provides a good compromise between the low area occupancy of ripple carry adders (RCAs) and the high-speed performance of carry look-ahead adders (CLAs). In the existing literature, many flavors of carry select addition have been realized on both ASIC and FPGA platforms with ASIC implementations being predominant. CSLAs usually involve duplication of RCA structures with presumed carry inputs of binary 0 and binary 1 to enable parallel addition and thereby speed up the addition process. Carry select addition can also be performed by utilizing the common Boolean logic (CBL) shared between the sum and carry outputs of a full adder. Nevertheless, due to the serial cascading of full adder modules, the delay metric would not decrease although the area parameter would reduce. Formatter will need to create these components, incorporating the applicable criteria that follow. Further, optimizations at the device, gate levels, and realization styles have been carried out to reduce area, improve speed, and minimize the power-delay product of CSAs on the basis of semicustom and full-custom ASIC-style synthesis. Rather than realizing pure CSAs, hybrid architectures incorporating carry select and carry look-ahead structures have also been proposed to improve the design efficiency of CSAs. Overall, a survey of published literature reveals that CSAs have been widely implemented. CSAs constructed using pure carry select structures are called "homogeneous CSAs" and CSAs realized using a combination of carry select and carry look-ahead structures are labeled as "heterogeneous/hybrid CSAs."

Figure 1 depicts an 8-bit RCA, which is formed by a cascade of full adder modules. The full adder is an arithmetic building block that adds an augend and addend bit (say, a and b) along with any carry input (Carry_in) and produces two outputs, namely, sum (Sum) and carry overflow (Carry_out). Since there is a rippling of carry from one full adder stage to another, the propagation delay of the RCA varies linearly in proportion to the adder width. The CSA basically partitions the input data into groups and addition within the groups is carried out in parallel that is, the CSA is composed of partitioned and duplicated RCAs.

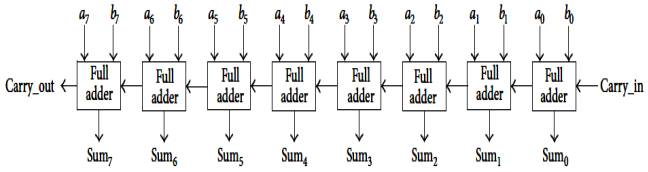

Figure 1: 8-bit RCA

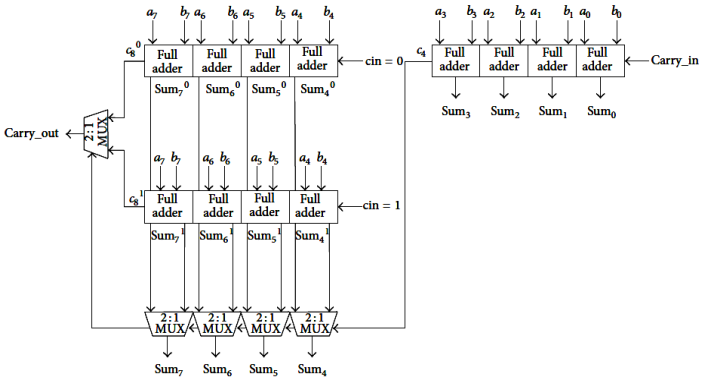

Figure 2: 8-bitCSA

Figure 2 shows the 8-bit conventional CSA comprising full adders and 2:1 MUXes, henceforth referred to as simply "CSA." In the case of CSA shown in Figure 2, the full adders present in the most significant nibble position are duplicated with carry inputs (c_{in}) of 0 and 1 assumed that is, one 4-bit RCA with a carry input (c_{in}) of 0 and another 4-bit RCA with a carry input (c_{in}) of 1 are used. Notice that both these RCAs have the same augend and addend inputs.

While the least significant 4-bit RCA would be adding the augend inputs (a_3 to a_0) with the addend inputs (b_3 to b_0), the more significant 4-bit RCAs would be simultaneously adding up the augend inputs (a_7 to a_4) with the addend inputs (b_7 to b_4), with presumed carry inputs (c_{in}) of 0 and 1. Due to two addition sets, two sets of sum and carry outputs are produced, one based on 0 as the carry input and another based on 1 as the carry input, which are in turn fed as inputs to the 2:1 MUXes. The number of MUXes used depends on the size of the RCA duplicated. To determine the true sum outputs and the real value of carry overflow pertaining to the most significant nibble position, the carry output (c_4) from the least significant 4-bit RCA is used as the common select input for all the MUXes, thereby the correct result corresponding to either the RCA with 0 as the carry input or the RCA with 1 as the carry input is displayed as output. Apart from the basic CSA with the help of RCA hybrid CSA architecture involve a Carry look-ahead adder with a intention of minimizing the maximum propagation path delay. Here carry look-ahead or section-carry based carry look-ahead adder is used. It is well known that a CLA is faster than a RCA, and hence it may be worthwhile to have a CLA as a replacement for the least significant RCA in the CSLA structure. Although the concept of carry look-ahead is widely understood, the concept of section-carry based carry look-ahead may not be that well known, and hence to explain the distinction between the two, sample 4-bit look-ahead logic realized using these two approaches is portrayed in Figure 3 for an illustration.

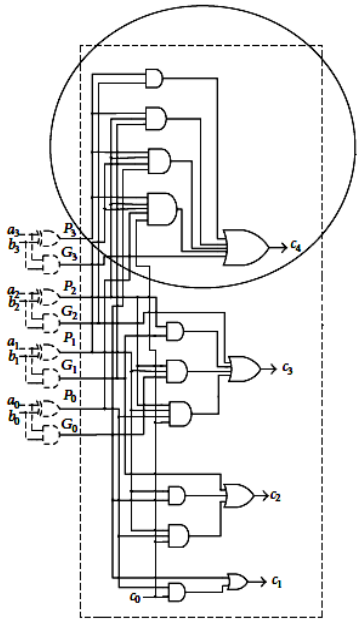

Figure 3: CLA

The section-carry based carry look-ahead generator shown enclosed within the circle in Figure 3 produces a single look-ahead carry signal corresponding to a "section" or "group" of the adder inputs (hence the term "section-carry"), while the conventional carry look-ahead generator encapsulated within the rectangle produces multiple look-ahead carry signals corresponding to each pair of augend and addend primary inputs. The section-carry based carry look-ahead generator differs from the traditional carry look-ahead generator in that bit-wise look-ahead carry signals are not required to be computed for the former. The XOR and AND gates used for producing the necessary propagate and generate signals (P_3 to P_0 and G_3 to G_0) are highlighted using dotted lines in Figure 3.

II. LITERATURE REVIEW

1) V. Kokilavani, K. Preethi,and P. Balasubramanian, "**FPGA-Based Synthesis of High-Speed Hybrid Carry Select Adders**" Hindawi Publishing Corporation Advances in Electronics Volume 2015, Article ID 713843.

Conclusion- CSLA is an important member of the high-speed adder family. In this paper, existing CSLA architectures viz. homogeneous and heterogeneous have been described and two new hybrid CSLA topologies were put forward: (i) carry select-cum-section-carry based carry look-ahead adder and (ii) carry select-cum-section-carry based carry look-ahead adder including BEC logic. The speed performances of the various CSLA structures have been analyzed based on the case studies of 32-bit and 64-bit dual-operand and multi-operand additions.

2) Basant Kumar Mohanty, Senior Member, IEEE, and Sujit Kumar Patel, "**Area–Delay–Power Efficient Carry-Select Adder**" IEEE Transaction on circuits and systems— II: express briefs , vol .61,no.6, Jun 2014.

Conclusion-This paper shows the analyzed n logic operations involved in the conventional and BEC-based CSLAs to study the data dependence and to identify redundant logic operations. They have eliminated all the redundant logic operations of the conventional CSLA and proposed a new logic formulation for the CSLA. In the proposed scheme, the CS operation is scheduled before the calculation of final-sum, which is different from the conventional approach.

3) Shivani Parmar, Kirat Pal Singh, "**Design of high speed hybrid carry select adder**," *IEEE Transactions on VLSI Systems,* 978-1-4673-4529-3/12 -2012

Conclusion-This paper proposed the efficient modified Carry Select Adder (CSA) of 8-bit, 16-bit, 32-bit and 64-bit word length by using a single Ripple Carry Adder (RCA).The selection of ripple carry adder gives the specifications by accurate resource estimation. The high speed carry select adder performs binary addition pervasive in FPGA applications. Modified carry select adder shows performance and resource improvements as compared with conventional carry select adder.

4) K. Preethi,and P. Balasubramanian, **"FPGA Implementation of Synchronou section-carry base carry look-ahead adder**" 2nd International conference on devices, circuits and systems (ICDCS), 2014 IEEE.

Conclusion-In this paper, FPGA based realization of high-speed carry look-ahead adders based on the concept of section-carry is discussed. Three kinds of carry look-ahead adder architectures viz. Type 1, Type 2, Mixed are presented. In comparison with conventional carry look-ahead adders of sizes 16, 32 and 64-bits, the proposed section-carry based carry look-ahead adders report improvements in speed of Type

1, Type 2 and Mixed topologies respectively, for simulations targeting a 90nm FPGA device.

5) Shamim Akhter, Saurabh Chaturvedi, Kilari Pardhasardi, "**CMOS implementation of efficient 16 bit square root carry select adder**" 2nd International Conference on Signal Processing and Integrated Networks (SPIN), 2015 IEEE.

Conclusion-In this paper, the SQRT (square root) CSA has been designed using CMOS TG technique. The TG based full adder blocks and multiplexers have advantage that there is no series critical path or longest path involved in the circuit like as in Manchester-chains, therefore CMOS TG technique is especially useful for low-power applications. The SQRT CSA balances well the area, power consumption and speed of performance.

III.CONCLUSION

From the above related papers, we come to the conclusion that the approximate propagation delay path of hybrid adder with RCA, CLA and CSA is 40 ns for 32-bit addition. Due to this, the performance speed of the configuration is affected. Hence, there is a need to reduce propagation path delay.
As the delay is matter for performance of the circuit, we will design a system that consumes a minimum delay.

REFERENCES

1) V. Kokilavani, K. Preethi,and P. Balasubramanian, "FPGA-Based Synthesis of High-Speed Hybrid Carry Select Adders" Hindawi Publishing Corporation Advances in Electronics Volume 2015, Article ID 713843.

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6) J.Monteiro, J. L. G¨untzel, and L. Agostini, "A1CSA: an energyefficient fast adder architecture for cell-based VLSI design," in Proceedings of the 18th IEEE International Conference on Electronics, Circuits and Systems (ICECS 11), pp. 442–445, Beirut, Lebanon, December 2011.