A NOVEL ARITHMATIC LOGIC UNIT DESIGN FOR DELAY & AREA OPTIMIZATION

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Abstract—In the modern era, speed and area of circuit under fabrication has become a major andvital constraint in electronic industry. For any digital system arithmetic and logic unit is the brain which used to perform basic arithmetic & logical operation. The objective of this project is to improve the delay which increases the speed of operation & faster system can be design. The purpose of this synopsis is the design and implementation of an Arithmetic Logic Unit (ALU) using area optimizing techniques such as Gate Diffusion Input (GDI) and Transmission Gate (TG). On the bases of review project we are designing 4bit-ALU by mix designing technique to reduce delay then conventional CMOS 4bit-ALU by using TANNER15.0 EDA tool.
This 4bit-ALU will design in 0.18µm technology with 1.8V supply voltage.

***Keywords*—**: GATE DIFFUSION INPUT, TRANSMISSON GATE, ALU,

I. INTRODUCTION

Arithmetic logic unit (ALU) is the basic block of central processing unit(CPU). Itis a crucial and core component of central processing unit as well as of numerous embedded system and microprocessor. ALU getting smaller nowadays and more complex nowadays to enable the development of a powerful but smaller computer. In the era of growing technology and scaling of device up to nanometer regime, the arithmetic logic unit circuits are to be designed with compact size, less power and propagations delay. Arithmetic operations are insensible and basic function for any high speed low power application digital signal processing, microprocessor, image processing etc. addition is most important part of the arithmetic unit rather approximately all other arithmetic operation include addition. Thus, the primary issue in the design of any arithmetic logic unit is to have low power high performance adder cell. There are various topologies and methodologies are proposed to design full adder cell efficiently. This technique designutilize the concept of GDI technique in the design of ALU and its sub blocks as Multiplexer and Full adder.very compact. It is frequently used in an array of processing elements on VLSI chips. This project uses 0.18µm technology for designing ALU where Delay willreduce, with supply voltage 1.8V and simulation will carried on TANNER EDA 15.0 tool.

1.1 GATE DIFFUSION INPUT TECHNIQUE

Morgenshtein has proposed basic GDI cell shown in Fig.1this is a new approach for designing low power digital combinational circuit.GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design

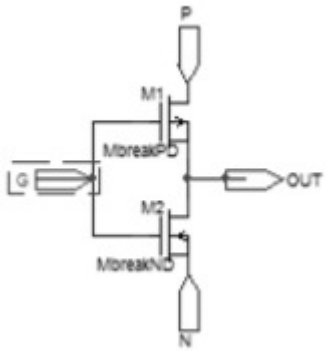

Fig. 1 BASIC GDI CELL

There are three inputs in a GDI cell - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N and P respectively. Table 1 shows different logic functionsimplemented by GDI logic [8] based on different input values. So, various logic functions can be implemented with less power and high speed with GDI technique as compared to conventional CMOS design.

CMOS Transmission Gate consists of the NMOS & PMOS connected in parallel. The gate voltage applied (input) to both transistor are set to be complimentary to each other.

CMOS TG work as a bidirectional switch between the Node input and output which is controlled by A. Shown in fig 2.
If the Controlled signal is logic high i.e. Vdd the both transistor turn on and provide a low resistance current path between the input and output. In other hand if the control signal is low which is 0 then both transistor will be off and path between A and B will be open circuit. So it is also called as high impedance state.

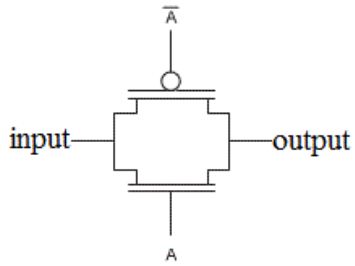

Fig. 2 Transmission Gate

II. LITERATURE REVIEW

The designing of high performance analog integrated circuits is becoming most essential with the continues trend toward the reduced supply voltage and and transistor channel length. MOS is the most success among all because it can be scaled down to smaller dimensions for higher performance. The size can be reduced to micrometer or nanometer for getting higher performance

1] Vivechana Dubey and RaviohanSairam**"An Arithmetic and Logic Unit optimized for**
Area and Power" 2014IEEE Forth International Conference On Advance Computing & communication technology

This paper based on 0.25µm CMOS technology is used with 1.8V power supply and simulation is done using TANNER EDA 13.0 simulator using TSMC BSIM. In this 4-bit ALU is design to meet the low power and minimum area. In today's CMOS circuits dynamic power dissipation is the main factor which causes power dissipation in CMOS circuits. So in this paper number of power supply to ground are reduced in GDI implementation which reduces the dynamic power consumption. Whole representation of ALU is design by GDI technique& various topologies of multiplexers and full adder implementation Is studied and compared. The 2x1 mux, 4x1 mux, 1-bit full adder with 10-transistor designed using GDI technique is chosen for lowering power consumption and minimum area. After simulation number of transistor for 4bit-ALU with CMOS gate- 592, ALU with transmission gate and 10 transistor full adder- 416 & Proposed 4bit-ALU with GDI based full adder- 232.
Power Consumption:- 4bit-ALU
Number of CMOS gate- 4204.5µW
ALU with transmission gate and
10 transistor full adder- 1197.5µW
Proposed 4bit-ALU withGDI based full adder-1030.5µW.

2] Shobha Mohan, Nakkeeram Rangaswamy **"Performance Analysis of 1 bit Full Adder Using GDI Logic"** ISBN no.978-1-4799-3834-6/14/$31.00©2014 IEEE

In this paper 1bit-full adder is designed by Gate Diffusion Input techniques using 120nm CMOS technology with corresponding voltage of 1.2V supply voltage The simulation result are compared with Pass transistor, Transmission function, and CMOS based adder circuits. The adder schematics are developed using DSCH2 CAD tool, In this paper new proposed design is made in which full swing operation by the use of one transistor is at output which leads to minimum power consumption.
The proposed design reduces the number of transistor in 1 bit full adder which is equal to 21transistors for normal CMOSFA need 28transistor.
Also it reduces the delay in circuit which is 18ps & previously for CMOS FA 27ps. But in case of power consumption proposed circuit does not settable power consumption increases in proposed circuit from 7.9µW to 9µW.

3] ArkadiyMorgenshtein, Alexander Fish, and Israel Wanger**"Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits"** 1063-8210-02$17.00©2002 IEEE

In this paper Gate Diffusion Input techniques use for design of basic gates which reduces power consumption, propagation delay and area of digital circuit while maintaining low complexity of logic design. The basic GDI cell operation is carried out from this paper. Using GDI technique various component are design such as 8-bit adder, 8bit-comaprator, 4-bit multiplier and all this designs compared with TG and CMOS circuits with respect to power consumption, propagation delay, transistor count. Performance comparison were done by simulating in cadence Spectre at Vdd =5v, $f$clk=10MHz, 1.6µm CMOS technology.

4]KrishnenduDhar, Anandchatterjee**"Design of an energy efficient, high speed, low power full sub tractor using GDI technique"**Department of electronics and telecommunication Engineeringjadavpur university, Kolkata India

This paper proposes the design of an energy efficient, high speed and low power full subtractor using Gate Diffusion Input (GDI) technique. The entire design has been performed in 150nm technology and on comparison with a full subtractor employing the conventional CMOS transistors, transmission gates and Complementary Pass-Transistor Logic (CPL) and transmissions gate.
The simulation of theproposed design has been carried out in Tanner SPICE and the layout has been designed in Microwind.In this paper found that there is a considerable amount of reduction in Average Power consumption (Pavg), delay time as well as Power Delay Product (PDP). Pavgis as low as 13.96nW while the delay time is found to be 18.02pico second thereby giving a PDP as low as 2.51x10-19 Joule for 1 volt power supply. In addition to this there is a significant reduction in transistor count compared to traditional fullsubtractoremploying CMOS transistors.
Transistor required for design:-
Number of transistor in full substract or for CMOS :– 50
Number of transistor in full substract or for Transmission gate :– 38
Number of transistor in full substract or for Complimentary pass transistor: – 34
Number of transistor in full substract or for Gate diffusion input :– 14

5] Arvind Kumar **"Comparative Study of 4-Bit ALU using CMOS and BiCMOS for 200nm Technology"**
Dept. of Electronics and communication , UIET, Punjab University, Chandigarh

In this paper, the design of a high performance 4-bit ALU using CMOS &BiCMOS technologies for high speed applications. These were further compared w.r.t. speed, power dissipation and power delay product. The comparison of CMOS to BiCMOS often seen in the literature shows the delay of single stage circuits driving a capacitive load, with the BiCMOS circuit exhibiting a bold advantage. TANNER EDA tools were used for schematic simulation.
The simulation technology used was MOSIS 200nm. This ALU can be used in mixed signal processing like radar system, image recognition, high speed broadband networks etc. The analog input signal must first be sampled and digitized using an ADC (analog to digital converter). The resulting binary numbers, representing successive sampled values of the input signal, were transferred to the processor. The ALU of the processor carried out numerical calculations with them. These calculations typically involve multiplying the input values by constants and adding the products together.
Comparative Study on each operation is performed for 4 bit ALU. Delay, number of transistor and power delay product are also compared to CMOS and BiCMOS.

III.CONCLUSION

From the above related paper, we come to the conclusion that as the numbers of power supply to ground connection are more so transistor dissipated morepower. To reduce Power Consumption GDI is efficient technique it reduces the number of power supply to ground connections which reduces minimum power consumption and minimum area to implement design. This GDI technique used to design Full adder circuits in ALU.

As the delay is matter for speed of processor so for minimum delay Transmission gate is used. The advantage of transmissions gate in some circuit can be explained by the fact that one nMOS and one pMOS transistor is conducting at once for each logic state in transmission gates. So TG can used for designing the multiplexer circuit in the ALU.

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