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DESIGN AND IMPLEMENTATION OF QPSK MODULATOR USING DIGITAL SUBCARRIER

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ABSTRACT : *The digitally implemented QPSK modulator is developed for satellite communication for future satellite missions. As we know that for space application power and bandwidth are most important parameters. The size of PCB and component count are also important parameters. To reduce these all parameters we design new approach. The new approach also minimizes the component count and hence reduces the PCB size. In this modulator summation, orthogonal sub-carrier generation and mixing of subcarrier with data are all digitally implemented inside the FPGA. Earlier, each of these functions were being implemented by external analog components which are frequency and temperature sensitive. So the components count was also more and leading to bigger PCB size. Therefore we design this new concept to remove all limitations of today's modulator circuits which are used in on board processing system. Digital approach for implementation of QPSK Modulation is attempted here. Realization of hardware blocks like CCITT V.35 Scrambler, Differential Encoder, ½ rate Convolutional Encoder, Sine and Cosine subcarrier generation, assignment of symbols with respect to I and Q data, their additions to obtain QPSK stream are digitally implemented inside an FPGA using suitable high frequency sampler. Exhaustive simulation and characterization are done to freeze design parameters. Only at the last end, the digital QPSK stream is converted to analog using 10 bit Digital to Analog Converter. Finally, the modulated signal obtained from D/A Converter is suitably translated to required carrier frequency.*

KEY WORDS : QPSK, NCO, FPGA, Digital Implementation, LVDS, LUT.

I. INTRODUCTION

In satellite communication , modulation is necessary to transfer the information between satellite and the earth. There are basically two types of modulation technique :ANALOG MODULATION and DIGITAL MODULATION. From these two modulation technique digital modulation technique have several advantages over analog modulation technique like less interference, greater fidelity, robust, high S/N ratio etc. So in satellite communication generally digital modulation is used .In digital modulation technique, there are several types of modulation techniques are present like ASK(Analog shift Keying), FSK(Frequency Shift Keying) , PSK(Phase Shift Keying) etc. All these have own advantages and disadvantages.

In satellite communication power, bandwidth and size of circuit are very important parameter. These parameter must be maintained for on board processing system in satellite communication. Now in satellite communication power is severally limited. For the satellite communication FSK is not generally used as it would require very high bandwidth to modulate our data resulting in very low bandwidth efficiency. Higher constellation QAM also cant be used in satellite communication as that would require very high C/N ratio. The choice is between QPSK and BPSK. The advantage of BPSK is that it requires the lowest C/N ratio. The drawback is that the data rate achieved using BPSK is very low. QPSK is basically two BPSK links operating on the same radio channel with their carriers in phase quadrature. Therefore the BER of a QPSK remains the same as BPSK. At the same time the data rate is doubled. MSK is also one type of PSK technique, but for this we require complex circuit and higher bandwidth than QPSK . Our project demands high data rate without losing much on bandwidth and power. Because of these trade offs we decided on using QPSK modulation scheme for application of satellite communication.

Now today in satellite communication for on board processing system QPSK modulator is used but in this modulator analog components are used like local oscillator, mixer, 90° phase shifter. All these components are frequency and temperature sensitive. Also the no of components are higher so size of PCB require for this modulator is comparatively high. So after few years the performances of these components are degrade. And ultimately this effects on the performance of QPSK modulator and this degrades the performance of satellite communication. So our aim to design such a modulator circuit which eliminates all these limitations of today's modulator circuit used in satellite communication. Here we design completely digital QPSK modulator. In our circuit we eliminate the use of local oscillator, mixer, 90° phase shifter. The functions of all these components are performed by FPGA. Here carrier is digitally generated using LUT(Look Up Table). Now FPGA is digital component which is frequency and temperature insensitive. So the

performance of this modulator can not degrade as time passes. And also the number of components are reduced and ultimately size of PCB is reduced. So all the limitations of today's modulator which are used in satellite communication are eliminated.

II. BLOCK DIAGRAM OF DIGITALLY IMPLEMNTED QPSK MDULATOR

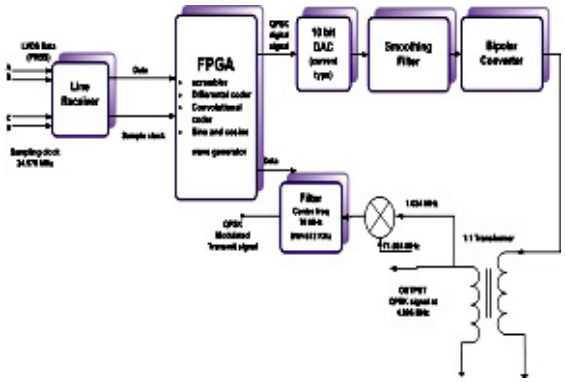

Figure: Basic Block Diagram of Digitally QPSK Modulator

A. LVDS DATA WITH LINE RECEIVER

LVDS is the abbreviation of Low Voltage Differential Signaling. It is an electrically digital signaling standard that can run at very high speed over inexpensive twisted pair copper cables. It specifies the electrical level in detail. Here, differential signaling means , it transmits information as the difference between the voltages on a pair of wires, two wire voltages are compared at line receiver. It is a dual wire system which can running at 180°of each other. so noise to travel at the same level, which in turn can get filtered more easily and effectively. In our project we use DS90C032 3V LVDS Quad CMOS Differential Line receiver.

B. FPGA

This block is heart of QPSK modulator. In this approach all the main operations to develop QPSK signal are perform by FPGA. Here our motive is to provide complete digital system and miniaturization of circuit so this can be done using FPGA. Here we provide only two Inputs, one is our information and second is the sample clock. We get the Digital QPSK signal from the FPGA. The internal functions of FPGA is Data scrambling, Differential coding, Convolutional encoding, Carrier generation, mixing the data with carriers and finally generate complete QPSK signal.

In this project we concentrate to use the ProASIC3E FPGA devices part no:A3PE600. This FPGA is satisfy the criteria of our application. All the features of FPGA is suitable to space requirements.

C. DAC(DIGITAL TO ANALOG CONVERTER)

As Block diagram, the output of FPGA is Digital QPSK signal. It means we get the samples of QPSK signal. To construct analog signal from this we must use Digital to analog converter. Here we use 10-bit current type DAC. In our project we use 10-bit, 170 MSPS, AD9731 DAC.

D. SMOOTHING FILTER

Digitally modulated QPSK samples out from DAC is a stair case type. There need to be smoothened by a smoothing filter to have a analog look of the modulated signal. The center frequency is 1.024 MHz with symbol rate 512 K bits/s, in order to preserve the main lobe while smoothing. The cutoff frequency of the filter has to be taken care of so that the main lobe is not affected but a smoothing do take place This filter is design using AADE filter design V4.5 tool. For our application we develop fifth order Butterworth low pass filter.

E. BIPOLAR CONVERTER

The DAC output is current type with an offset in the -ve direction because the DAC output is ECL type. We know that PSK or QPSK is suppressed carrier modulated system. Carrier suppression is possible only if there is no DC in the data, this requires conversion of QPSK samples to be converted into bipolar type so that there is no overall DC so bipolar converter circuit serve this purpose.

III. SUB CARRIER GENERATION USING FPGA

As per our main aim summation, orthogonal sub-carrier generation and mixing of subcarrier with data are all digitally implemented inside the FPGA. Here, LVDS data is used and this data are given to he scrambler and than ½ rate FEC coder is used. All this blocks are present inside the FPGA. For this blocks, the modules are develop in verilog language using Xilinx tool.

The main part is generation of carriers means sine and cosine signals. These signals are generated at 1.024 MHz. These signals are generated inside the FPGA using the quantized value of samples of both signals.

There are several techniques to generate sine and cosine wave digitally. Its called NCO (Numerically Controlled Oscillator). There are several techniques to implement NCO

1. LUT Based NCO
2. CORDIC Based NCO
3. Xilinx ROM Based NCO

Among all these we implement LUT based NCO for our application. In this technique a NCO consists of a lookup table made up of quantized sinusoidal sample values(usually implemented as a read only memory, ROM), a binary counter for addressing the ROM, and

a clock signal to drive the counter as shown in below figure.

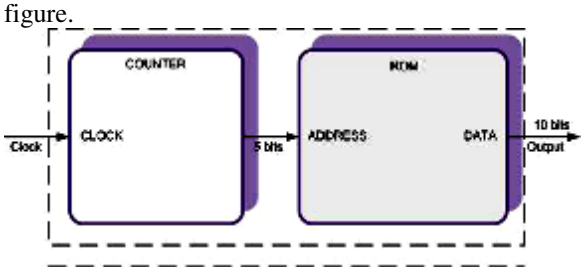

Figure:2 A Numerically Controlled Oscillator

Successive address locations in the ROM contain the successive quantized sample values of the desired sinusoid signals. As the counter is clocked, each new count addresses the next ROM location causing the appropriate digital number to appear at the ROM output. The rate at which the counter is clocked is the sample rate of the system. The number of bits in the ROM's output word determines the resolution of the desired digital sinusoid.

In our application we need 9 bit output from NCO then using twos-complement representation would yield a numeric range of -361 to +361 for the amplitude values of our quantized sampled sinusoid signals.

Many variations on this theme can be found in the literature. The main point is that a NCO serves as a means for generating a digital sinusoid at a specific sample rate but with programmable frequency. The frequency is restricted, however, to an integer multiple of the sample rate divided by the ROM word length up to a maximum of ½ of the sample rate (the Nyquist constraint). The larger the ROM length (address range), the finer the frequency resolution. The more bits in the ROM output word, the finer the amplitude resolution.

III. SIMULATION RESULTS

A. SPECIFICATION

Modulation	QPSK
Carrier Frequency	70 MHz
Data Rate	512 Kbps
Symbol Rate	256 Kbps
Sub carrier frequency	1.024 MHz
Sub carrier quantization	10 bits
Amplitude imbalance	0.4 dB(max)
Phase imbalance	within 3°
Scrambler	CCITT V.35
Input signal Interface	LVDS
Phase Ambiguity Removal	By differential coding

B. FLOW DIAGRAM OF MATLAB SIMULATION

The flow diagram gives the steps to perform the simulation of digitally implemented QPSK modulator in MATLAB.

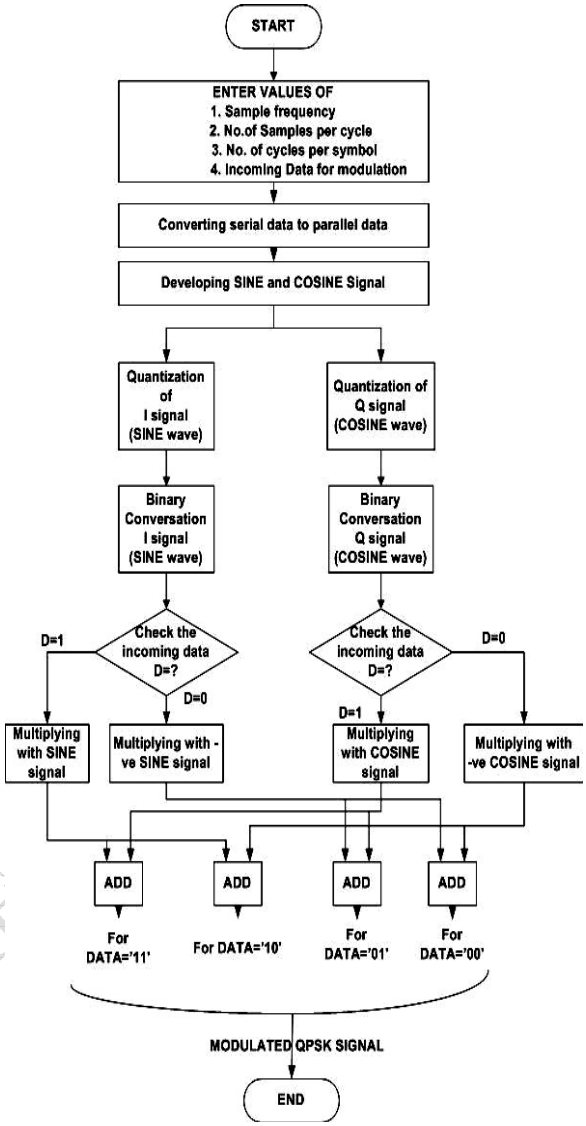

Figure:3 Flow diagram of MATLAB simulation

C. MATLAB SIMULATION RESULTS

As per flow diagram COSINE and SINE carriers for I and Q data respectively are generated. Here the sub carriers with frequency 1.024 MHz and 24 samples per cycle are generated. There are 4 cycles per symbols are necessary to modulate incoming data. These carriers are first multiplex with the I and Q data and than added together in single FPGA. In following simulation results the subcarriers per symbol, the final QPSK modulated signal and its frequency spectrum are given

The subcarrier generation per symbol is given in below figure:.

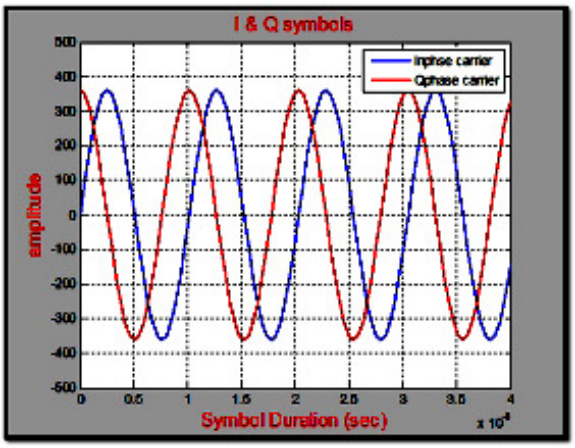

Figure:4 Subcarrier generation of carrier per symbol

Now, This carrier is ready to modulate. The data 1100' is given for modulation. This data is first converted into parallel form and individual data is multiply with either cosine or sine carrier like BPSK. After that these individual modulated data is added together and QPSK modulated signal is generated The simulation result for time domain representation of QPSK signal is given in below figure:

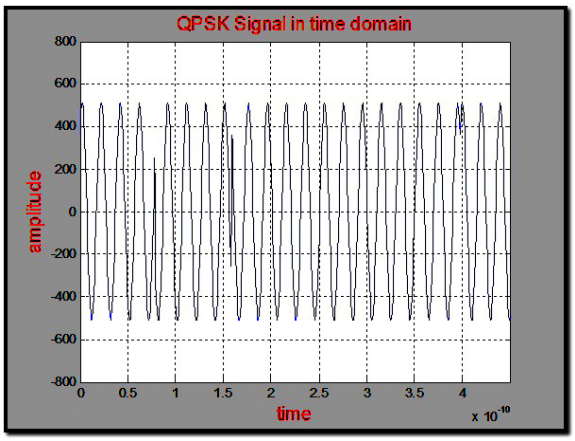

Figure:5 Time domain representation of QPSK signal

Frequency Domain Representation for QPSK signal is:

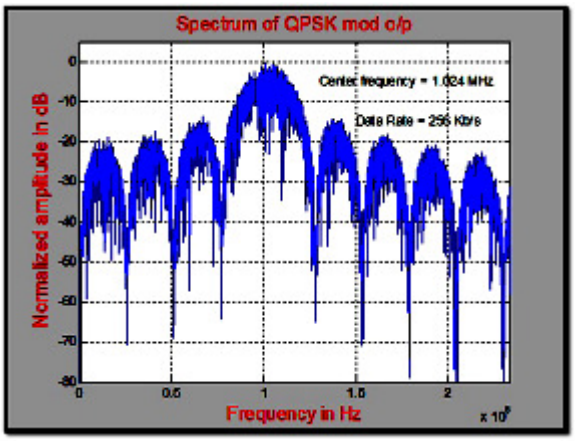

Figure:6 Frequency domain representation of QPSK signal

IV. HARDWARE REALIZATION

In hardware realization we use Actel kit with ProASIC3000 FPGA. In this kit we load our program which is written in verilog. The Actel Kit is shown below:

Figure:7 Actel ProASIC 3000 kit

The output of kit is shown in logic analyzer. Here in Actel kit Scrambler, Differential encoder, Convolutional coder and subcarrier generator are implemented. The setup of this implementation with results are shown below. And as per output which is shown in figure there is no phase and amplitude imbalance between sin and cosine subcarriers.

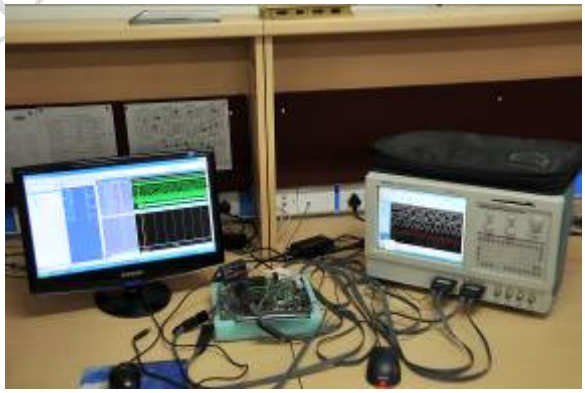

Figure:7 Set up of digitally implemented QPSK modulator

V. ACKNOWLEDGEMENT

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VI. CONCLUSION

Here, we design digitally QPSK modulator. In this modulator , analog components like local oscillator and mixer are completely eliminated which are frequency and temperature sensitive. Here all the functions are performed by single FPGA. So the limitations of modulator are completely removed for satellite communication. For the satellite communication PCB size is also important parameter and using this new approach number of component count is less and ultimately size of PCB is become small.

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