

# 125 KHz RFID SYSTEM

<sup>1</sup> MR.ROHAN NITIN PRADHAN, <sup>2</sup> FALGUN AJAY SHAH, <sup>3</sup> RAHUL NIRMAL ARYA  
<sup>4</sup> KASHISH M MAKHIJANI(Guide)

<sup>1,2,3</sup> Students of Electronics & communication Dept., Babaria Institute of Technology,  
Varnama, Vadodara, Gujarat, India

<sup>4</sup> Assi prof. Electronics & communication Dept., Babaria Institute of Technology,  
Varnama, Vadodara, Gujarat, India

*rohan.pradhan@rocketmail.com, falgunshah96@yahoo.com, rahulNarya@gmail.com*  
*makhijani.kashish@gmail.com*

**ABSTRACT : ABSTRACT.** Radio Frequency Identification (RFID), one of the key technologies of silent commerce has been gaining momentum over the past couple of years. One area that is widely benefited from the use of RFID is supply chain management. A huge spectrum of benefits will be unlocked when adoption across the entire supply network is realized. These benefits would eventually ripple through all industries and sectors and open up a host of additional applications that will benefit both the corporate and civilian community. The main focus of this paper will be on the designing of the interrogator that will support the new RFID network in various applications. "The core idea of the paper is reducing the problem faced while designing A RFID INTERROGATOR and problem faced TO READ ITS TAGS".

Simulation results have been shown and discussed in brief using Multisim Simulation Software to show how circuit could be tested before hardware implementation

**KEYWORDS:** Multisim; RFID reader; transmitter; Backscattering modulation; receiver; virtual tag

## 1: INTRODUCTION

Our future in communication systems is more challenging as the innovation is the only way out and its efficiency will depend on what we as engineers can contribute. In fact, our future depends on such systems and their accuracy is a must for us. For testing of such systems companies had developed much simulation software. It is based on the process of modeling a real phenomenon with a set of mathematical formula. It is, essentially, a program that allows the user to observe an operation through simulation without actually performing that operation.[1] Simulation software is used widely to design equipment so that the final product will be as close to design specs as possible without expensive in process modification.

Radio-frequency identification (RFID) is a technology that uses communication via electromagnetic waves to exchange data between a terminal and an electronic tag attached to an object, for the purpose of identification and tracking.[1,2] Some tags can be read from several meters away and beyond the line of sight of the reader. Radio-frequency identification involves interrogators (also known as readers), and tags (also known as labels). Most RFID tags contain at least two parts. One is an integrated circuit for storing and processing information, modulating and demodulating a radio-frequency (RF) signal, and other

specialized functions. The other is an antenna for receiving and transmitting the signal.

Nowadays RFID systems are used for asset management, inventory control, security system, animal tracking, keyless entry, automatic toll debiting. RFID is wireless, means non-contacting technique range from inches to feet. Tag and reader can be reusable as it is programmable device. The RFID tags have been normally used at many ISM band frequencies from KHz to GHz. Here testing of the system circuits becomes very easy using MULTISIM software.

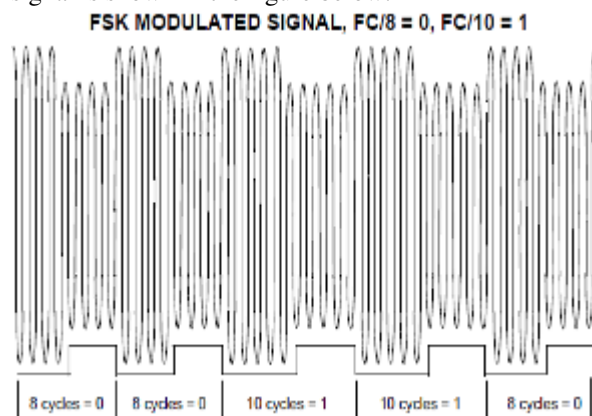
## 2 : DESCRIPTION

The RFID system consists of reader and tag. There are three types of RFID tags: passive RFID tags, which have no power source and require an external electromagnetic field to initiate a signal transmission, active RFID tags, which contain a battery and can transmit signals once an external source ('Interrogator') has been successfully identified, and battery assisted passive (BAP) RFID tags, which require an external source to wake up but have significant higher forward link capability providing greater range.

Presently we are dealing with passive tags, Tag consists of a silicon device and antenna circuit. The purpose of the antenna circuit is to induce an energizing signal and to send a modulated RF signal. The read range of tag largely depends upon the antenna circuit and size. The antenna circuit of tag is made of LC resonant circuit or E-field dipole antenna, depending on the carrier frequency. The LC resonant circuit is used for the frequency of less than 100 MHz. In this frequency band, the communication between the reader and tag takes place with magnetic coupling between the two antennas through the magnetic field. The antenna utilizing the inductive coupling is often called magnetic dipole antenna. The antenna circuit must be designed such a way to maximize the magnetic coupling between them. This can be achieved with the following parameters:

- a) LC circuit must be tuned to the carrier frequency of the reader
- b) Maximize Q of the tuned circuit
- c) Maximize antenna size within physical limit of application requirement.

Our tag uses FSK modulation. This form of modulation uses two different frequencies for data transfer; the most common FSK mode is FC/8/10. In other words, a '0' is transmitted as an amplitude-modulated clock cycle with period corresponding to the carrier frequency divided by 8, and a '1' is transmitted as an amplitude-modulated clock cycle period corresponding to the carrier frequency divided by 10. The amplitude modulation of the carrier thus switches from FC/8 to FC/10 corresponding to 0's and 1's in the bit stream, and the reader has only to count cycles between the peak-detected clock edges to decode the data. FSK allows for a simple reader design, provides very strong noise immunity, but suffers from a lower data rate than some other forms of data modulation. Here our FC is 125KHz and FC/10 is 12.5KHz which is logic '1' and FC/8 is 15.625KHz which is logic '0'. The FSK modulated signal is shown in the figure below:

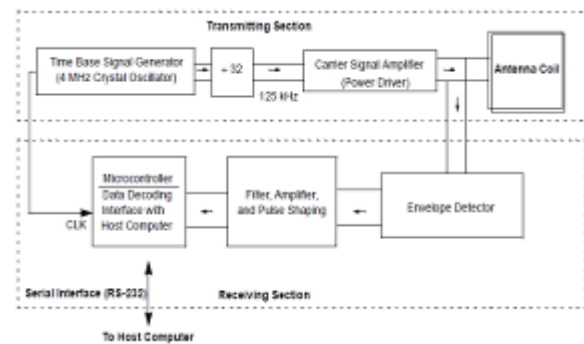


The reader circuit should provide 125 KHz carrier signal to the tag and detect the modulated signal via Backscatter modulation. This terminology refers to the communication method used by a passive RFID tag to send data to the reader using the same reader's

carrier signal. The incoming RF carrier signal to the tag is transmitted back to the reader with tag's data. The RF voltage induced in the tag's antenna is amplitude-modulated by the modulation signal (data) of tag device. The changes in the voltage amplitude of tag's antenna can effect on the voltage of the reader antenna. By monitoring the changes in the reader antenna voltage (due to the tag's modulation data), the data in the tag can be reconstructed. The modulation done to the signal can be seen in the figure above.

The block diagram for our reader can be found in the figure below:

**BLOCK DIAGRAM OF TYPICAL RFID READER FOR FSK SIGNAL (125 kHz)**

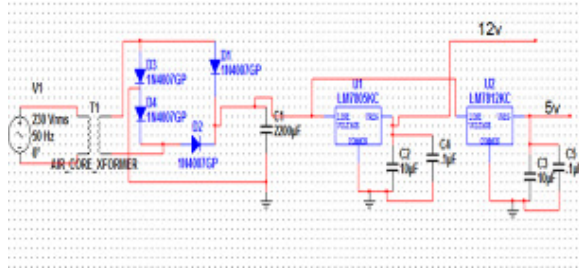


Our RFID interrogator/reader is divided into the following parts in our circuit simulation.

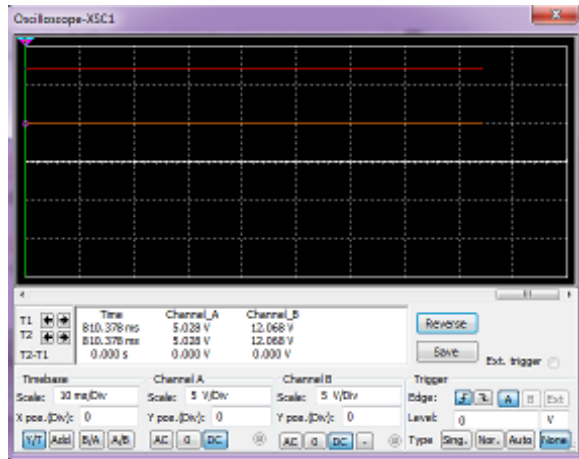
- (1) Power supply-our circuit requires 5v and 12v supply in various stages.
- (2) Transmitter stage-It is used for generation of 125KHz square wave and getting sine wave by passing through the RF inductor and is used for power amplification of the carrier generated.
- (3) Antenna stage-It is used for transmitting and receiving the signals and to provide power to the passive tag by the radiated carrier signal itself.
- (4) Filter stage-This stage includes envelope detector to obtain the modulated signal due to back scatter modulation. And to minimize the noise content.
- (5) Comparator stage-This stage converts the obtained modulated signal from analog to digital.
- (6) Counter stage- This stage is used to remove the ripple and to avoid the crippling of the system.
- (7) Virtual Tag-it is the emulation of the original tag.

Schematic Designs & Simulated Inputs &Outputs

A. Power Supply:



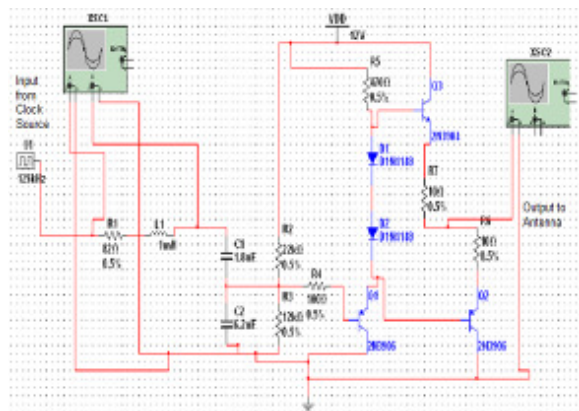
Output:



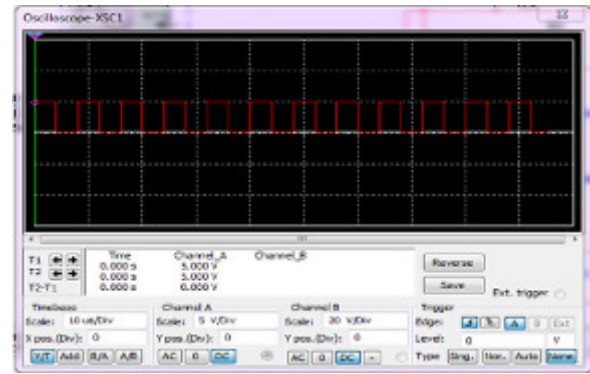
Our simulation is working perfectly fine for generating 5v & 12v supply

B. Transmitter Stage

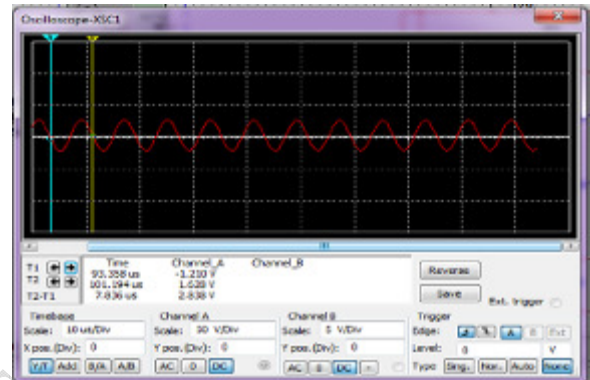
The circuit in figure below starts with a square wave generator of 125 KHz, we can use counter or microcontroller for generation in practical. After it an RLC filter followed by a power amplifier is used. The RLC filter is used to filter out most of the upper harmonic frequencies present in the square wave, leaving our fundamental frequency, 125 KHz sine wave. This sine wave is further amplified to boost the transmitting signal level by the power amplifier as shown in schematic below. A complementary push-pull amplifier is used as power amplifier & preceded by the tuning circuits to match the impedance of the transmitter to the characteristics of the antenna.



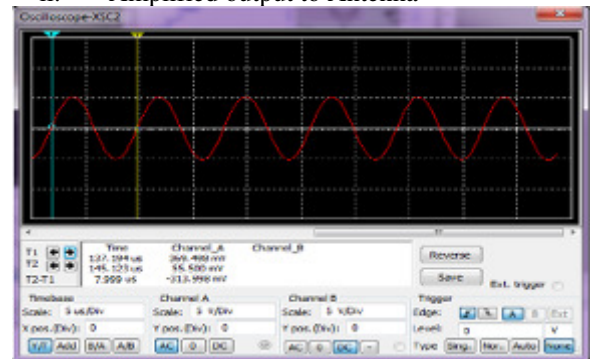
input square wave of 125khz



i. Generation of sinewave through RLC Filter.



ii. Amplified output to Antenna



iii. Calculation:

Here, we can see that outcome is giving a sine wave at the end of the power amplifier stage. The frequency of the sine wave is found out to be 125 KHz by T1 and T2 from the above figure.

$$f = \frac{1}{T_2 - T_1}$$

$$= \frac{1}{7.999 \mu s}$$

$$= 125.01 \text{ KHz}$$

C. Antenna & Detector stage

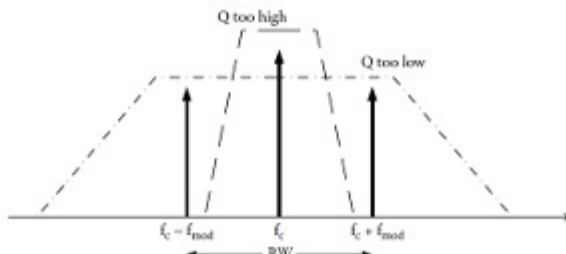
Here Antenna chosen consists of only LC. But our entire readers heart is the antenna ,if it doesnt work

well, our reader won't work well. Here the value of L and C is decided by the equation:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

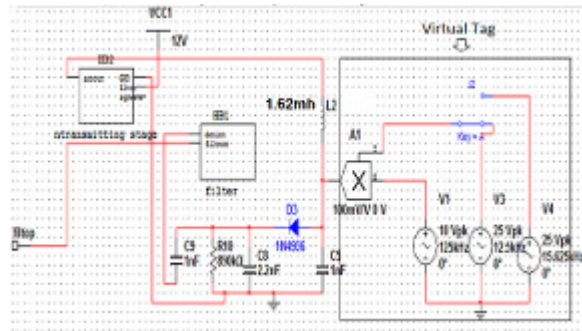
here  $f_0$  is the fundamental frequency (in Hertz), L is inductance (in Henries) and C is capacitance (in Farads). Here Fundamental frequency = 125 KHz and we used 1 nF ceramic capacitors, and found an inductance of 1.62 mH. This inductance is chosen to get Q-factor 20.

A high Q-factor indicates an antenna that is very narrow in frequency, that is, very narrow in frequency i.e. highly selective. This may be good in order to reject interfering signals that otherwise would be detected by the antenna. However RFID signal has a certain bandwidth. If antenna is too selective, it may distort the components of the transmitted signal that fall outside the selectivity of the antenna as shown in figure below. A good compromise is to choose a Q-factor around 20.

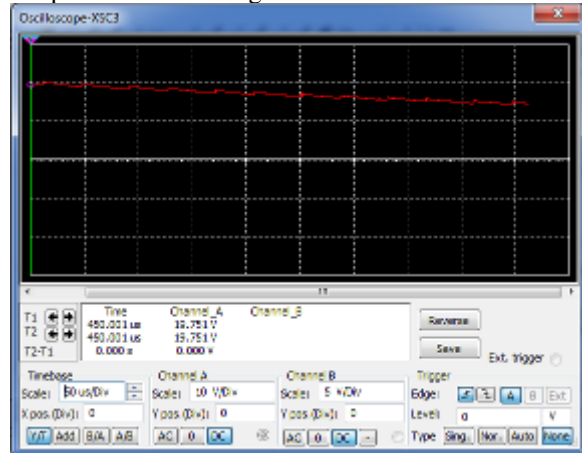


Detector stage: The first step is demodulating the backscattering signal obtained from antenna, and the second step is detecting the frequency (or period) of the demodulation signal. The demodulation is accomplished by detecting the envelope of the carrier signal. A half-wave capacitor-filtered rectifier circuit is used for the demodulation process. A diode detects the peak voltage of the backscattering signal. The voltage is then fed into an RC charging/discharging circuit. The RC time constant must be small enough to allow the voltage across C to fall fast enough to keep in step with the envelope. However, the time constant must not be so small as to introduce excessive ripple. The demodulated signal must then pass through a filter. For this we chose  $R=890\text{Kohms}$  and  $C=2.2\text{nF}$  as shown in the schematic.

Antenna & detector stage schematic:

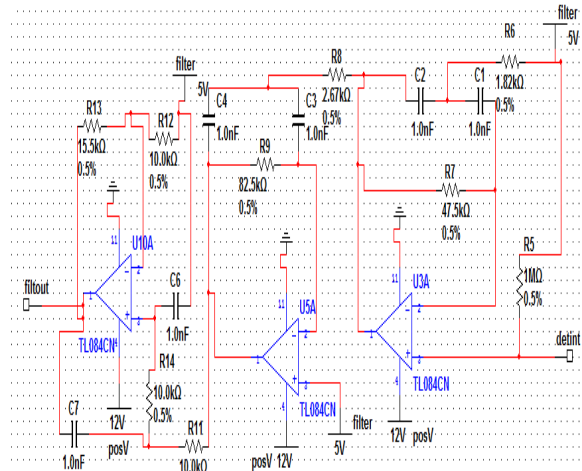


Output of Detector stage:

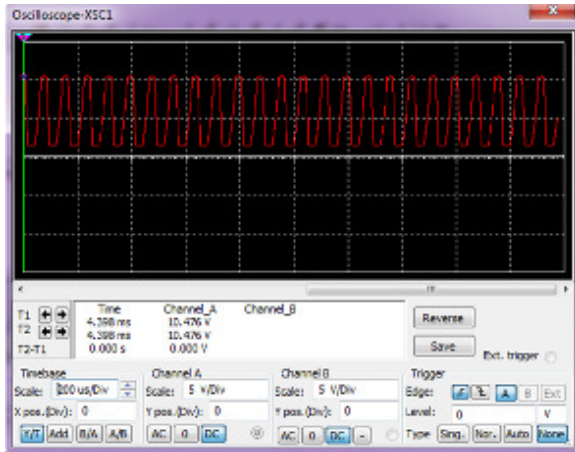


#### D. Filter stage

The detected signal from the envelope is sent to the filter circuit, here we need to extract two frequencies one is 12.5KHz and 15.625KHz for logic 1 and logic 0 respectively from the backscattering signal, we need to remove the ripples from this frequencies and provide proper pulse wave shaping to it. [1] For it we used opamp-TL084 as the active Butterworth filters as shown in the schematic below:

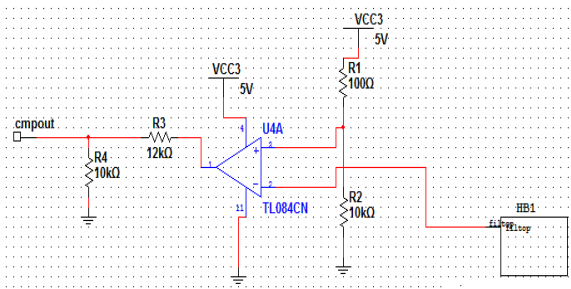


Filter output:

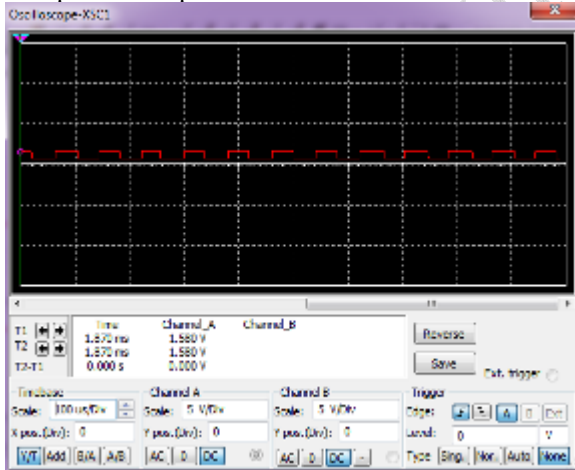


E. Comparator stage

After filtering, the signal is made to pass through a comparator and followed by resistive divider to convert the analog into digital for understanding of controllers. This conversion creates square waves for 12.5 KHz and 15.625 KHz frequencies coming out of pulse shaping circuit.[1]



Comparator Output for 12.5KHz



Similarly we can find it for 15.625 KHz by switching the virtual tag.

F. Counter stage

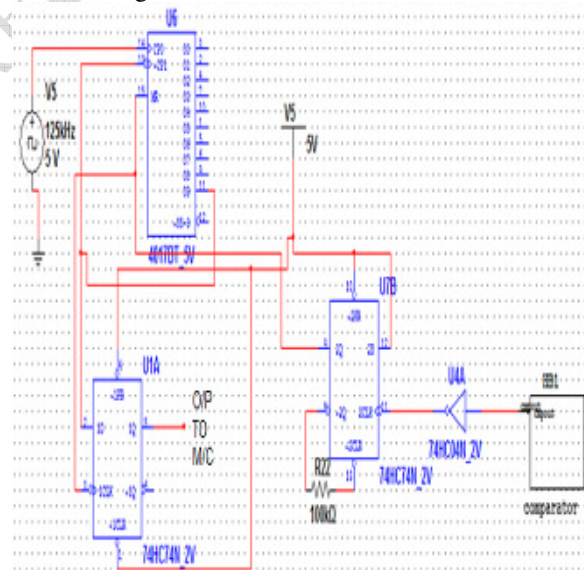
As such we should have been able to read the data from the comparator directly. But we found out that doing this would lead to more problems in the programming stage. For this we found a extremely good idea of using dual D-flip flop with the decade counter as shown in the schematic below. The Basic idea of using this stage is to get logic 1(high) for 12.5KHz frequency and logic 0 (low) for 15.625 kHz

directly and not having to interpret square waves of 12.5KHz and 15.625KHz frequencies for logic 1 and 0 respectively. Thus we can directly just read the bits for logic 1 and 0 via the microcontroller leaving it only to decode the data from the tag.

The working of the circuit is as follows, we give the output of comparator at one of the D-flip flops as the clock source and giving +5v to the d input and to the set input of the flip-flop .Here as we can see from the schematic below we have given the ~q output to the clear input of the flip-flop via the 100kohm resistor, it is used for generation of short pulse. Here with the help of counter we are sampling 125KHz, here we find that our requirement of 12.5KHz =125/10KHz can be found on pin 9 of the counter i.e. if we see output of pins, we get at pin 0, 100000000, at pin 1, 010000000, and so on. At pin 9 we get 12.5KHz.Now the incoming short pulse from the output of first d flip-flop will reset the counter before the pin 9 can activate if the incoming pulse from the comparator is other than that of 12.5KHz.Then the output of pin 9 is given to the input of second flip flop as well as to its clock source.

This takes care that the output of second flip-flop remains at logic 1 if pin 9 is activated and thus gives logic 1 for 12.5KHz, otherwise the output of second flip-flop remains at logic 0 serving our purpose.

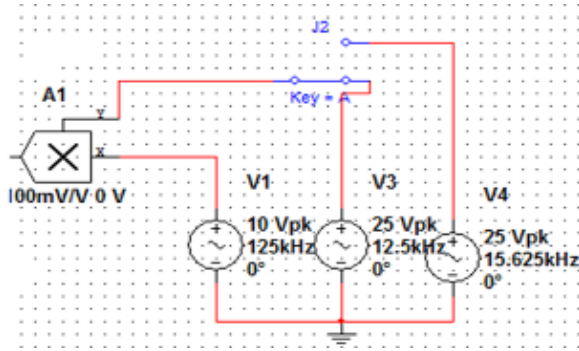
Counter stage:



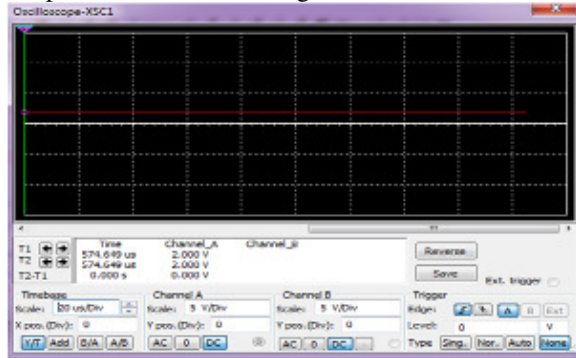
Counter output:

Counter output will vary according to the modulating frequency given by the tag.i.e

- a. Virtual Tag at 12.5khz

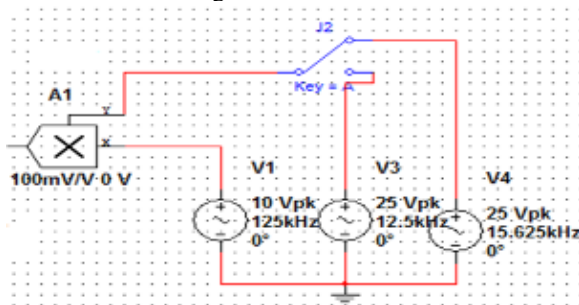


Output for 12.5kHz i.e. Logic 1

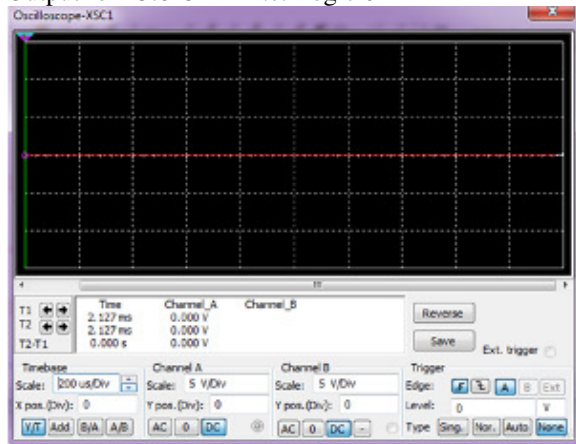


Here we can see that we are getting logic 1 for 12.5khz.

b. Virtual Tag at 15.625khz



Output for 15.625kHz i.e. Logic 0



Here we can see that we are getting logic 0 for 15.625khz.

G. Data retrieval stage.

The output of comparator is given to a microcontroller for reading the data. The obtained encoded data has to be decoded. Data encoding refers to processing or altering the data bitstream in-between the time it is retrieved from the RFID chip's data array and its transmission back to the reader. The various encoding algorithms affect error recovery, cost of implementation, bandwidth, synchronization capability and other aspects of the system design. Entire textbooks are written on the subject, but there are several popular methods used in RFID tagging today:

1. NRZ (Non-Return to Zero) Direct. In this method no data encoding is done at all; the 1's and 0's are clocked from the data array directly to the output transistor. A low in the peak-detected modulation is a '0' and a high is a '1'.
2. Differential Biphas. Several different forms of differential biphas are used, but in general the bitstream being clocked out of the data array is modified so that a transition always occurs on every clock edge, and 1's and 0's are distinguished by the transitions within the middle of the clock period. This method is used to embed clocking information to help synchronize the reader to the bitstream. Because it always has a transition at a clock edge, it inherently provides some error correction capability. Any clock edge that does not contain a transition in the data stream is in error and can be used to reconstruct the data.
3. Biphas\_L (Manchester). This is a variation of biphas encoding in which there is not always a transition at the clock edge.

SIGNAL	WAVEFORM	DESCRIPTION
Data	1 0 1 1 0 0 0 1 1 0 1 0	Digital Data
Bit Rate CLK		Clock Signal
NRZ_L (Direct)		Non-Return to Zero - Level '1' is represented by logic high level. '0' is represented by logic low level.
Biphase_L (Manchester)		Biphase - Level (Split Phase) A level change occurs at middle of every bit clock period. '1' is represented by a high to low level change at midclock. '0' is represented by a low to high level change at midclock.

Here manufacturers of tag uses weigand protocol for the security along with the one of the encodings described above. Now though wiegand protocol is standard of 26,34 bits.but manufacturers have started using their own protocols for the security of cards so that tags data becomes readable only to certain

reader modules. To decode the code of any tag using the above reader circuit we need to detect the three to four tags of the same manufacturer, check the incoming bits on the hyper terminal using the microcontroller and remove the repeating bits appearing in all the three and the remaining bits would be our encoded data. Further this encoded data can be decoded by testing for the encoded form used in it .

#### **H. Tradeoffs:**

Here we have used more of hardware than software, but we can do reduce the hardware by using more of software i.e. Using microcontroller having inbuilt comparator, we can reduce our stages till filter only, but this will lead to more sensitive programming.

### **3: CONCLUSION**

Through this paper we have tried to simulate the whole RFID Interrogator using Simulation software .The results shows that the simulation is working perfectly for 125KHz frequency but the whole set of RFID frequencies can be generated using the same software. The Hardware implementation of the same is what we would be working as a future work.

### **4: REFERENCES**

- [1]Albert Lozano-Nieto ,”RFID Design Fundamentals and Applications,”2011 Taylor and FrancisGroup,LLC,pp.86-154.
- [2]MicrochipTechnologyInc,microID@125 kHzRFID System Design Guide, 2004, pp.1-7,98 -112.
- [3] Probabilistic RFID Data Management Nodira Khossainova, Magdalena Balazinska, and Dan Suciu Department of Computer Science and Engineering University of Washington Seattle, WA June 20, 2007
- [4]A. Deshpande, C. Guestrin, and S. R. Madden. Using probabilistic models for data management in acquisitional environments. In Proc. of the Second Biennial Conference on Innovative Data Systems Research (CIDR), Jan. 2005.
- [5]RFID in operation and supply chain management by Thorsten Bleckerand George Q Huang EVS .info/