COMPLEXITY IN DESIGNING OF LOW NOISE AMPLIFIER

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ABSTRACT: *Amplifiers play a critical role in a Communication System. They are used to increase the voltage, current, and/or power of a signal, in both transmitters and receivers. LNA is used at the front end of the receivers. Important properties of amplifiers include gain, input and output impedances measured using S-parameters, noise figure, stability, bias networks, interface with other circuits (ports). When designing a linear narrow band amplifier, the goal is to produce a design that is well matched at the design frequency and has a good gain and low noise at that frequency. The S-parameters are a function of bias condition, so the result using a set of S-parameters are only valid at the bias conditions at which the S-parameters were measured or simulated. In this Paper, using bilateral approach LNA is designed using RF transistor BFP 540 (product of Infineon Technology). The BFP 540 gives maximum gain with moderate noise figure by keeping VSWR $_{in}$ as constant whereas, plot of VSWR (input/output) variations are observed separately.*

Keywords— Low noise amplifier, Stability, Matching Networks, Noise Figure, VSWR, Bilateral Design, DC bias Network.

I: INTRODUCTION

In Communication System LNA (low noise amplifier) provides first level of amplification of the signal received at the system's antenna. It plays an undisputed important role in the receiver design. Its main function is to amplify extremely low signals without adding noise, thus preserving required signal to noise ratio of the extremely low power levels and for large signal levels, it amplifies the received signal without introducing any distortions, hence eliminating channel interference. The most important design considerations in a LNA design are stability, power gain, bandwidth, noise figure, VSWR and DC requirement.

II: KEY FEATURES FOR LNA DESIGN

1. Selection of a proper transistor by examining datasheets.
2. Checking the conditional stability of transistor.
3. Biasing is selected depending on the application like low power, low noise, high power ,linearity, etc.
4. Different techniques are applied to optimize different parameters. Two parameters cannot be optimized simultaneously.
5. Matching circuits that provide optimum performance in a microwave amplifier can be easily and quickly designed using a Smith Chart. Lumped components are replaced with distributed transmission lines.
6. In the design of a LNA, the transistor should have minimum intrinsic noise. Noise sources present in a transistor should be properly modeled.

III: CONSIDERABLE COMPLEXITY IN LNA DESIGN

LNA design presents a considerable complexity because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. All these parameters are interdependent and do not always work in each other's favour. Carefully selecting a transistor and understanding parameter limitations can meet most of these conditions. Low noise figure and good input match can be obtained using feedback arrangements. Unconditional stability will always require a certain gain reduction because of either shunt or series resistive loading of the collector. There is a major limitation to observe variations in VSWR parameters. It is not possible to plot input and output VSWR circles simultaneously. A Plot of (Input / Output) VSWR shows that one of the network is matched properly and it is considered as reference to observe variation in the other side of the network.

IV: STABILITY CONSIDERATIONS

The stability of an amplifier, or its resistance to oscillate, is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. Instabilities are primarily caused by three phenomena (1) Internal feedback of the transistor, (2) External feedback around the transistor caused by external circuit, or (3) Excess of gain at frequencies outside the band of operation. To determine the stability of a device, calculate the Rollett's stability factor (K) using a set of S-parameters given for the device at the frequency of operation. K and $|\Delta|$ give us an indication to whether a device is likely to oscillate or not or whether it is conditionally/unconditionally stable.

The parameter must satisfy $K > 1$ and $|\Delta| < 1$ for a transistor to be unconditionally stable.

In terms of reflection coefficients, the conditions for unconditional stability at a given frequency are
$|\Gamma_L| < 1$, $|\Gamma_S|$ $\Delta = S_{11}S_{22} - S_{12}S_{21}$

$$|\Gamma_{in}| = \left| \frac{S_{11} - \Gamma_L \Delta}{1 - S_{22}\Gamma_L} \right| < 1$$

$$|\Gamma_{out}| = \left| \frac{S_{22} - \Gamma_S \Delta}{1 - S_{11}\Gamma_S} \right| < 1$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1$$

The unconditionally stable conditions can be represented graphically also. The graphical analysis is especially useful in the analysis of potentially unstable transistors. The active device would be showing unconditional stability, as there is no intersection of the stability circles on the Smith Chart as shown in figure 1. Thus, the device will be stable for all possible matches on the input or output of the active device. Figure 2 shows the second case where S_{11} or $S_{22} > 1$ the origin is the part of the unstable region. When S_{11} or $S_{22} < 1$, the origin is part of
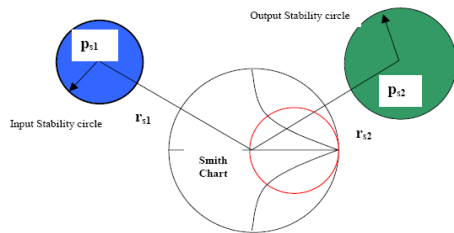

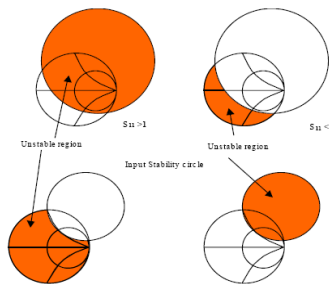Figure 1 Stability Circles for Unconditional Stability

Figure 1 Area of Stability for Conditional Stability

V: DESIGN OF THE INPUT AND OUTPUT MATCHING SECTIONS
1. **Input matching network**: It minimizes the noise influence. It is employed to match the input of the transistor to the source to provide a noise figure F as close to F_{min} as possible over the amplifier band width.
2. **Output matching network**: It maximizes power handling capabilities. It is required to match the output of transistor to the load to provide the highest possible gain. There are

two ways to obtain desired gain (1) Unilateral case (2) Bilateral case.

Unilateral Case: To obtain a desired gain performance, the influence of the transistor's feedback is neglected. ($S_{12} \approx 0$)

Bilateral Case ($S_{12} \neq 0$): For practical application, in bilateral design feedback effect is considered to overcome the error introduced in unilateral design where feedback is not considered. ($S_{12} \approx 0$)

Thus, the purpose of a matching network can be defined as a transformation to convert given impedance value to another more suitable value. Figure 3 illustrates a typical situation in which a transistor, in order to deliver maximum power to the $Z_o = 50 \, \Omega$ load, must have the terminations Z_S and Z_L.
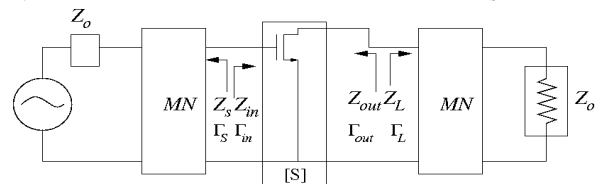

Figure 2 Block diagram of Microwave Amplifier

The network with strip lines and stub sections are more suitable for operational frequencies exceeding 1 GHz. With increasing frequency and corresponding reduced wavelength, the influence of parasitic in the discrete elements becomes more noticeable and taking their effect complicating the component value computations. As an alternative to lumped elements, distributed components are widely used when the wavelength becomes sufficiently small compared with the characteristic circuit component length. Even, it is easy to fabricate in micro strip or strip line form with a microwave fabrication aspect, since lumped elements are not required. To minimize the size of the circuit board, try to employ the shortest possible transmission line segments.

Particularly, in this paper for designing matching network, single stub in shunt form, balanced stub and impedance transforming properties of transmission lines are used. The shunt component can be open/short-circuit stub lines depending on the impedance requirements. The single stub in shunt form is shown in figure 4.The impedance matching networks can be designed either mathematically or graphically with the aid of Smith Chart. Here, graphical approach of ZY Smith Chart is used in the design of matching networks.
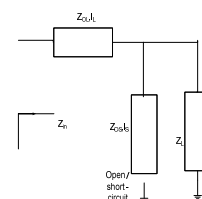

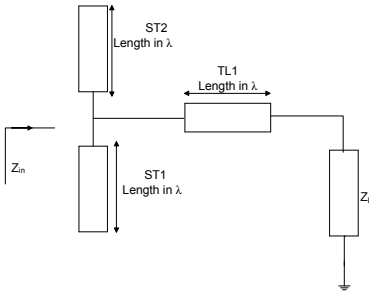Figure 3 Single Stub Matching Network

Figure 4 Balanced Stub Matching Network

In practical realizations single sided unbalanced stubs are replaced by the balanced stub along the series transmission line (TL1) to minimize transition interaction between the shunt stubs and the series transmission lines as shown in figure 5.Two parallel shunt stubs ST1 and ST2 must provide the same admittance as the single stub. Therefore, the admittance of each side of the balanced stub must be equal to half of the total admittance. It is important to note that the length of the shunt stubs is not equal to the total length of the balanced stubs.

Impedance transforming properties of transmission line uses micro strip lines with different characteristic impedances. A micro strip line can be used as a series transmission line, as an open circuited stub or as a short circuited stub. A series micro strip line together with a short-or open circuited shunt stub can transform a 50 Ω resistor into any value of impedance. Also, a quarter wave micro strip line can be used to change a 50 Ω resistor to any value of resistance. This line, together with a short-or open circuited shunt stub, can be used to transform 50 Ω to any value of impedance.

VI: AMPLIFIER POWER GAIN RELATIONS

There are three basic important parameters for calculations of power gain. They can be defined as transducer power gain, operating power gain and available power gain. They depend upon the source, load, input, output reflection co-efficient and S-parameters. Bilateral design is considered as simultaneous conjugate match. When $S_{12} \neq 0$, and the unilateral assumption cannot be made. Solving input and output reflection equations to obtain the simultaneous conjugate match. They are known as matched source and load reflection coefficients respectively, Γ_{MS} and Γ_{ML} .

The maximum transducer gain G_T is given by

$$G_{T,\max} = \frac{(1-|\Gamma_{ML}|^2)|S_{21}|^2(1-|\Gamma_{MS}|^2)}{|(1-S_{11}\Gamma_{MS})(1-S_{22}\Gamma_{ML})-S_{21}S_{12}\Gamma_{ML}\Gamma_{MS}|}$$

Maximum gain is given by

$$G_{T\max} = \frac{|S_{21}|}{|S_{12}|}\left(K-\sqrt{K^2-1}\right)$$

Similarly, Operating power gain G_P can also be solved and it can be represented in circle equations to plot operating power gain circle.

VII: NOISE FIGURE

For RF amplifiers, the need for signal amplification at low noise level becomes an essential system requirement. As designing a low noise amplifier competes with factors as stability and gain. For instance, a minimum noise performance at maximum gain cannot be obtained. It is necessary to develop a method that allows us to display the influence of noise as part of the smith chart to conduct comparisons and observe trade-offs between gain and stability.

The noise figure circle can be represented as

$$F = F_{\min} + \frac{4R_n}{Z_o}\frac{|\Gamma_S - \Gamma_{opt}|^2}{(1-|\Gamma_S|^2)|1+\Gamma_{opt}|^2}$$

In above equation the quantities F_{min} (minimum noise figure), R_n (noise resistance of the device), Γ_{opt} (optimum source reflection coefficient) are known. Adjust Γ_S such that, $\Gamma_S = \Gamma_{opt}$ so that the lowest possible noise figure is achieved, $F=F_{min}$. The above equation is in the form which on the right hand side suggests the form of a circle equation. It can be solved to plot the noise figure circles. In a design there is always a difference between the designed noise figure and the measured noise figure of the final amplifier. This occurs because of the loss associated with the matching elements and the transistor noise figure variations from unit to unit.

VIII: VSWR PARAMETERS

The amplifier has to stay below a specified VSWR as measured at the input or output port of the amplifier. Typical values ranges between 1.5≤VSWR≤2.5. The purpose of matching networks is to reduce the VSWR at the transistor. The complication arises from the fact that the input VSWR ($VSWR_{IMN}$) is determined at the input matching network (IMN), which in turn is affected by the active device, and, through feedback, by the output matching network (OMN). Conversely, the output VSWR ($VSWR_{OMN}$) is determined by the OMN and, again through feedback, by the IMN. Figure 6 shows the block diagram for input and output VSWR.
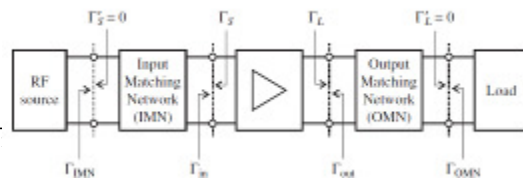

Figure 5 Block diagram for Input and Output VSWR

$$VSWR_{IMN} = \frac{1+|\Gamma_{IMN}|}{1-|\Gamma_{IMN}|} \quad VSWR_{OMN} = \frac{1+|\Gamma_{OMN}|}{1-|\Gamma_{OMN}|}$$

Above equations can be solved in form of circle equations to plot input/output VSWR circles. Under

bilateral matching the input and output reflection coefficients are the functions of source and load reflection coefficients (Γ_S, Γ_L).Therefore, the input and output VSWR circles cannot be plotted simultaneously, but rather have to be considered one at a time in the iterative process of adjusting Γ_S and Γ_L.

IX: DC BIAS NETWORK

An important building block in any RF circuit is the active or passive dc biasing network. The purpose of a good dc biasing is to provide the appropriate quiescent point for the active devices under specified operating conditions and maintain a constant setting irrespective of transistor parameter variations and temperature fluctuations. The biasing not only sets the DC operating conditions but must also ensure isolation of the RF signal through the use of radio frequency chokes (RFC) and blocking capacitors. In this LNA design, the dc biasing network with a bypassed emitter resistor is employed.

X: SIMULATION RESULTS FOR BILATERAL DESIGN AND CONCLUSION

Data for the RF Transistor BFP 540(Infineon Technology)

Operating Condition: $V_{ce} = 1$ V , $I_c = 12$ mA , f = 2.4 GHz, Gain=15.9 dB

$r_n = 0.10\ \Omega$, $F_{min} = 1.12$, $\Gamma_{OPT} = 0.20\angle -146°$

S-Parameters:

$S_{11} = 0.4933\angle 166.3°$	$S_{12} = 0.0846\angle 40.5°$
$S_{21} = 5.388\angle 63.5°$	$S_{22} = 0.1980\angle 126.5°$

Stability , Gain and noise figure Results

K	Δ	G_T (dB)	Actual NF(dB)
1.122	0.5521	15.914	1.5161

VSWR parameters

$VSWR_{in}$	$VSWR_{out(min)/(max)}$
1.2	1/1.25

Calculation of Reflection Coefficients for simultaneous conjugate match for matching network

Γms	Γml
-0.5529-0.1140i	0.0319+0.1641i
y_{ms}	y_{ml}
3.2+1.0708i	0.8903-0.3006i

Plot of Stability Circles, Operating Power Gain Circles for Maximum Gain, Noise Figure and VSWR Circle as follows:
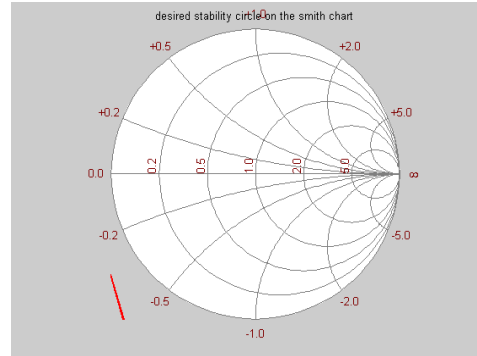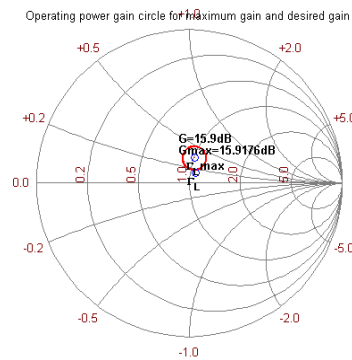

Figure 6 Stability Circles

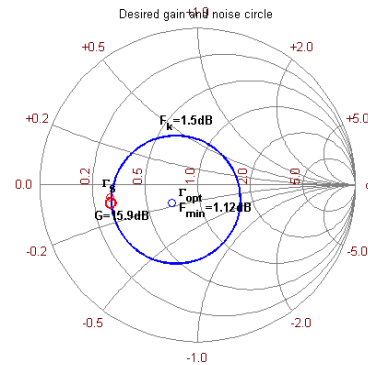Figure 7 Operating Power Gain Circles
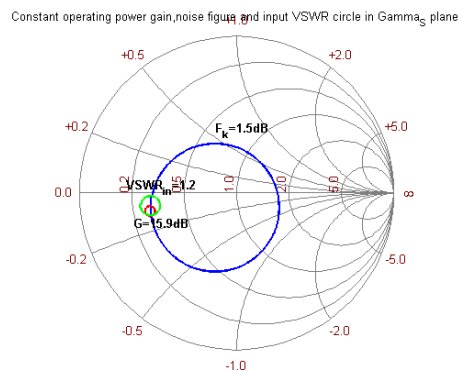

Figure 9 NF=1.5 dB and Max. Gain=15.9 dB

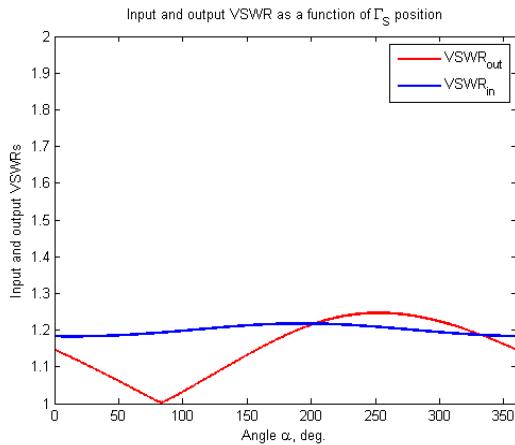Figure 10 VSWR$_{IN}$= 1.2, NF=1.5 dB, Max. Gain=15.9 dB circle

Figure 11 Input and Output VSWR plot (For VSWR$_{in}$=1.2, min VSWR$_{out}$ = 1/max. VSWR$_{out}$=1.2)

Circuit Realization and Draw backs: The dc biasing network with a bypassed emitter resistor is employed as shown in below figures. It provides the passive biasing to the RF BJT. The bypass capacitor C$_e$ is typically 0.01 µF disk capacitors. The RFC are typically made of 2 or 3 turns of No.36 enameled wire on 0.1 in. air core. The chip capacitors C$_A$ are coupling capacitors having typical values 200 to 1000 pF. The bypass capacitors C$_B$ are chip capacitors having typical values of 50 to 500 pF. The typical value of h_{FE} is 100. The Stability factors are S_i = 7.769, S_{hFE} = 9.23*10^{-6}, S_{VBE} = -9.23. Matching networks are designed with the help of smith chart for maximum gain 15.9dB. MATLAB result shows that moderate noise figure can be obtained for maximum gain, but it is difficult to realize the VSWR effect. VSWR plot shows that by keeping one parameter constant, other parameter variations can be realized.
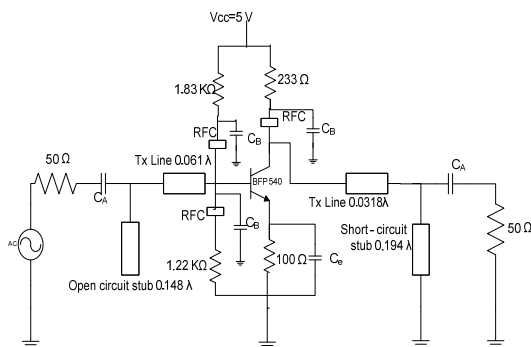

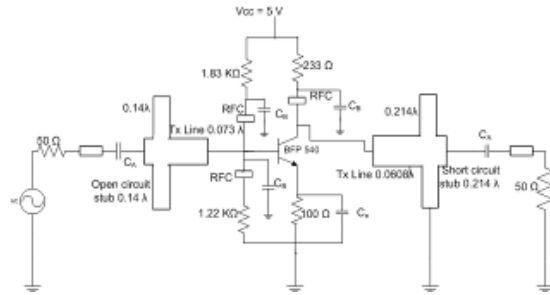Figure 12 Amplifier Schematic of BFP 540 (Single Stub)

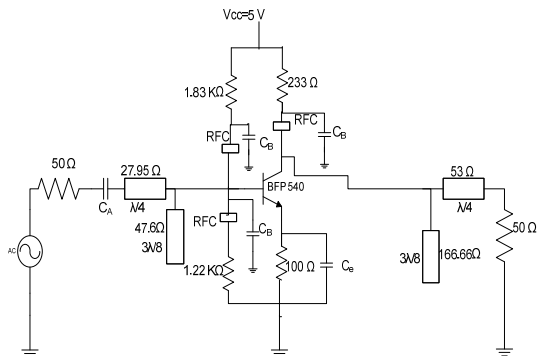Figure 13 Amplifier Schematic of BFP 540 (Balanced Stub)

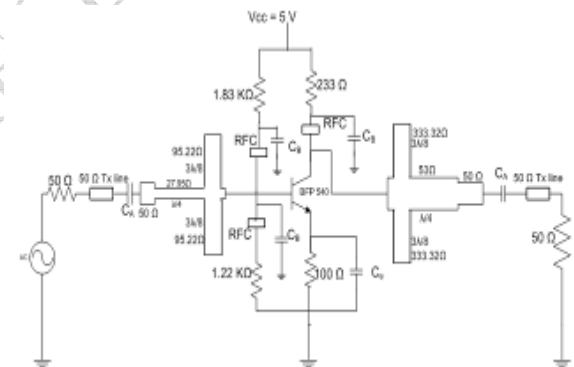Figure 14 Amplifier Schematic of BFP 540 (Single Stub using different characteristic impedance)

Figure 15 Amplifier Schematic of BFP 540 (Balanced Stub using different characteristic impedance)

Conclusion: Stability, gain, noise figure and VSWR performances are obtained using MATLAB. The matching circuits are calculated using Smith Chart. Three different networks are designed using single stub, balanced stub and impedance transforming properties of transmission lines. The DC bias circuit is designed with the help of voltage divider configuration. Some errors are likely to exist in the final implementation of the design resulting from parameter variations, stray capacitances and other random causes.

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