A Research Paper on Designing a TAP(Test Access Port)

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ABSTRACT *:TAP(Test Access Port) is fully boundary scanning technique to test the outer part of the ICs. The number of pins can be easily increased by following the instructions. Also the TAP contains instructions like Serial data input, Serial data output, test mode select, test clock and reset. The test cost can be reduced through less test time, less tester memory requirement, or a cheaper tester. The expected outputs will be as a test pattern will be given as a input and as expected output we are getting we can say if the test is passed or fail.*

KEYWORDS: TAP, TDI, TDO, TRST, TCK, BIST, TMS, Boundary Scan, CUT

1. PROBLEM STATEMENT

"To Design a Test Access Port for detecting defects at system and board level"

Objective:

To reduces cost of a Test.
To decrease the debug time.
To Reduces the fixture cost.
Also supports a chip, board and system level tests.

Scope:

This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to:
testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate.
testing the integrated circuit itself.
observing or modifying circuit activity during the component's normal operation.
The test logic consists of a boundary-scan register and other building blocks and is accessed through a Test Access Port (TAP).

Motivation:

Need to test for chip interconnect defects at the board level and to perform an internal chip test once it has been installed.
There is a need to determine whether all the components are installed correctly.
There is a need to control the whole boundary scan test procedure.
This aspect impacts the cost/time constraint and can be used elsewhere or on other devices. In addition, TAP can provide at speed, in system testing of the Circuit-Under- Test (CUT) . All these benefits are plentiful motivations for TAP.

2. INTRODUCTION

This TAP is a part of a boundary scan. And without this ports the boundary scan will become human without heart. Boundary Scan is a family of test methodologies aiming at resolving many test problems: from chip level to system level, from logic cores to interconnects between cores, and from digital circuits to analog or mixed-mode circuits. It is now widely accepted in industry and has been considered as an industry standard in most large IC system designs. Earlier, most Printed Circuit Board (PCB) testing was done using bed-of-nail in-circuit test equipment. Recent advances with VLSI technology now enable microprocessors and Application Specific Integrated Circuits (ASICs) to be packaged into fine pitch, high count packages. The miniaturization of device packaging, the development of surface-mounted packaging, double-sided and multi-layer board to accommodate the extra interconnects between the increased density of devices on the board reduces the physical accessibility of test points for traditional bed-of-nails in-circuit tester and poses a great challenge to test manufacturing defects in future.[1] In 1994, a supplement that contains a description of the boundary-scan Description Language (BSDL) was added to the standard. Since that time, this standard has been adopted by major electronics companies all over the world. But now a days the new HDL world called VERILOG coding, with using it we can now built the TAP and the boundary scanning.

Clearly the testing of mixed-mode circuits at the various levels of integration will be a critical test issue for the system-on-chip design. Therefore there is a demand to combine all the boundary scan standards into an integrated one.

3. BOUNDARY SCAN ARCHITECTURE

The boundary-scan test architecture provides a means to test interconnects between integrated circuits on a board without using physical test probes. It adds a boundary-scan cell that includes a multiplexer and latches, to each pin on the device. Figure 2.1 illustrates the main elements of a universal boundary-scan device.

The Figure 2.1 shows the following elements:

Test Access Port (TAP) with a set of four dedicated test pins: Test Data In (TDI), Test Mode Select (TMS), Test Clock (TCK), Test Data Out (TDO) and one optional test pin Test Reset (TRST*).
A boundary-scan cell on each device primary input and primary output pin, connected internally to form a serial boundary-scan register (Boundary Scan).
A TAP controller with inputs TCK, TMS, and TRST*.
An n-bit (n >= 2) instruction register holding the current instruction.
A 1-bit Bypass register (Bypass).
An optional 32-bit Identification register capable of being loaded with a permanent device identification code.

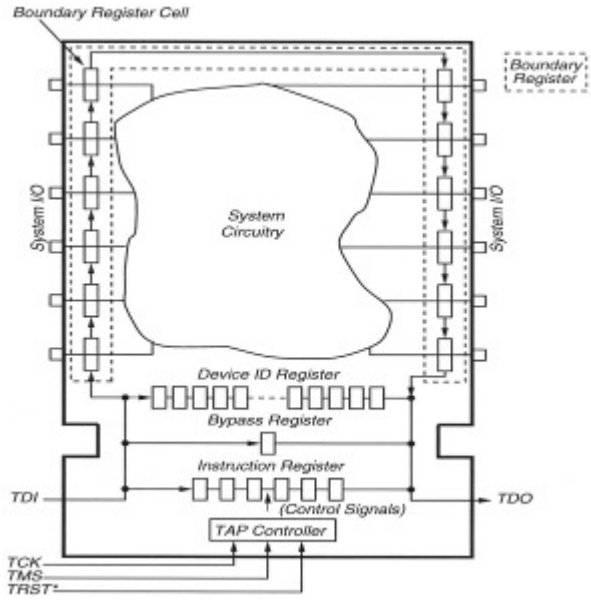

Figure 1 Basic Architecture

The test access ports (TAP), which define the bus protocol of boundary scan, are the additional I/O pins needed for each chip employing Std.1149.1a. The TAP controller is a 16-state final state machine that controls each step of the operations of boundary scan. Each instruction to be carried out by the boundary scan architecture is stored in the Instruction Register. The various control signals associated with the instruction are then provided by a decoder.

4. BUS PROTOCOL

The Test Access Ports (TAPs) are general purpose ports and provide access to the test function of the IC between the application circuit and the chip's I/O pads. It includes four mandatory pins TCK, TDI, TDO and TMS and one optional pin TRST* as described below. All TAP inputs and outputs shall be dedicated connections to the component (i.e., the pins used shall not be used for any other purpose)[3].

Test Clock Input (TCK): A clock independent of the system clock for the chip so that test operations can be synchronized between the various parts of a chip. It also synchronizes the operations between the various chips on a printed circuit board. As a convention, the test instructions and data are loaded from system input pins on the rising edge of TCK and driven through system output pins on its falling edge. TCK is pulsed by the equipment controlling the test and not by the tested device. It can be pulsed at any frequency (up to a maximum of some MHz). It can be even pulsed at varying rates.

Test Data Input (TDI): an input line to allow the test instruction and test data to be loaded into the instruction register and the various test data registers, respectively.

Test Data Output (TDO): an output line used to serially output the data from the JTAG registers to the equipment controlling the test.

Test Mode Selector (TMS): the test control input to the TAP controller. It controls the transitions of the test interface state machine. The test operations are controlled by the sequence of 1s and 0s applied to this input. Usually this is the most important input that has to be controlled by external testers or the on-board test controller.

Test Reset Input (TRST*): The optional TRST* pin is used to initialize the TAP controller, that is, if the TRST* pin is used, then the TAP controller can be asynchronously reset to a Test-Logic-Reset state when a 0 is applied at TRST*. This pin can also be used to reset the circuit under test, however it is not recommended for this application.

5. BOUNDARY SCAN CELL

Two mandatory test data registers, the bypass and the boundary-scan resisters, must be included in any boundary scan architecture.[2] The boundary scan register, though may be a little confusing by its name, refers to the collection of the boundary scan cells. The other registers, such as the device identification register and the design-specific test data registers, can be added optionally.

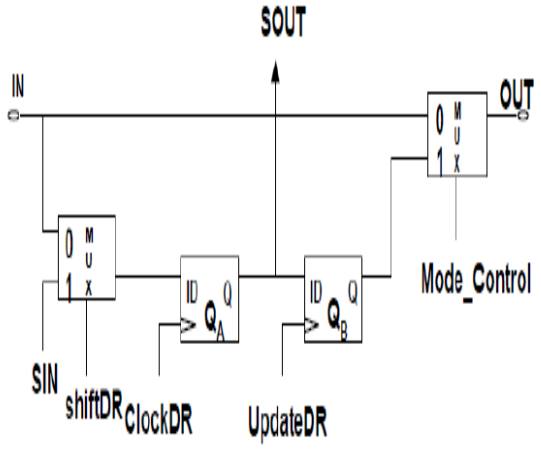

Figure 2 Boundary Scan Cell

Figure 2 shows a basic universal boundary-scan cell, known as a BC_1. The cell has four modes of operation: normal, update, capture, and serial shift. The memory elements are two D-type flip-flops with front-end and back-end multiplexing of data. It is important to note that the circuit shown in Figure 2.3 is only an example of how the requirement defined in the Standard could be realized.

The Standard does not mandate the design of the circuit, only its functional specification. The four modes of operation are as follows:

During normal mode also called serial mode, Data_In is passed straight through to Data_Out. During update mode, the content of the Update Hold cell is passed through to Data_Out. Signal values already present in the output scan cells to be passed out through the device output pins. Signal values already present in the input scan cells will be passed into the internal logic. During capture mode, the Data_In signal is routed to the input Capture Scan cell and the value is captured by the next ClockDR. ClockDR is a derivative of TCK. Signal values on device input pins to be loaded into input cells, and signal values passing from the internal logic to device output pins to be loaded into output cells During shift mode, the Scan_Out of one Capture Scan cell is passed to the Scan_In of the next Capture Scan cell via a hard-wired path.

6. BOUNDARY SCAN PATH

At the device level, the boundary-scan elements contribute nothing to the functionality of the internal logic. In fact, the boundary-scan path is independent of the function of the device. The value of the scan path is at the board level as Shown in Figure3.[3]

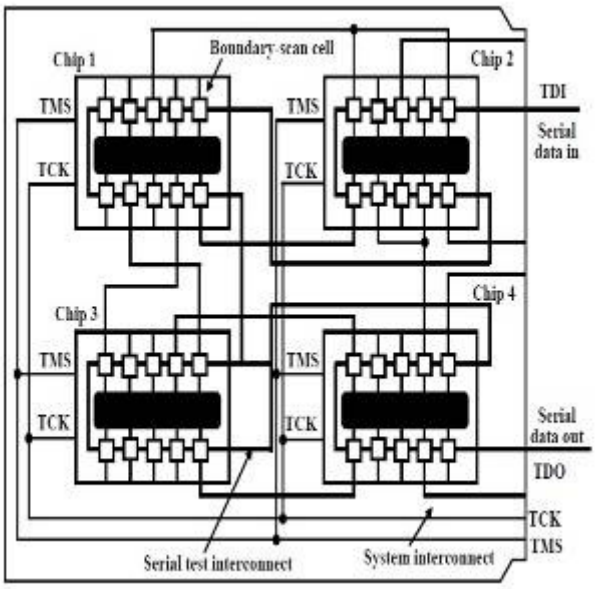

Figure 3 Boundary Scan path

7. TAP CONTROLLER

The operation of the test interface is controlled by the Test Access Port (TAP) controller. This is a 16-state finite state-machine whose state transitions are controller by the TMS signal; the state-transition diagram is shown in Figure 4. The TAP controller can change state only at the rising edge of TCK and the next state is determined by the logic level of TMS. In other words, the state transition in Figure 3 follows the edge with label 1 when the TMS line is set to 1, otherwise the edge with label 0 is followed. The output signals of the TAP controller corresponding to a subset of the labels associated with the various states. As shown in Figure 1, the TAP consists of four mandatory terminals plus one optional terminal.[1]

The main functions of the TAP controller are:

To reset the boundary scan architecture.

To select the output of instruction or test data to shift out to TDO.

To provide control signals to load instructions into Instruction Register.

To provide signals to shift test data from TDI and test response to TDO.

To provide signals to perform test functions such as capture and application of test data.

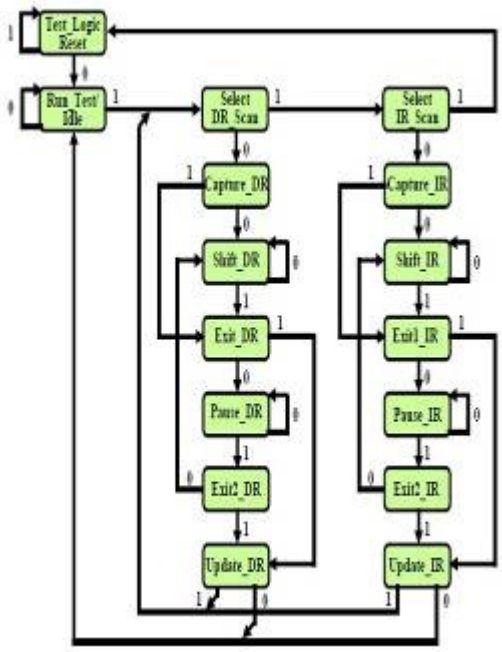

Figure 4 TAP Controller FSM

OPERATION

Figure 4 shows the 16-state state table for the TAP controller. The value on the state transition arcs is the value of TMS. A state transition occurs on the positive edge of TCK and the controller output values change on the negative edge of TCK. The 16 states can be divided into three parts.

The first part contains the reset and idle states, the second and third parts control the operations of the data and instruction registers, respectively. Since the only difference between the second and the third parts are on the registers they deal with, in the following only the states in the first and second parts are described. Similar description on the second part can be applied to the third part.

Test-Logic-Reset: In this state, the boundary scan circuitry is disabled and the system is in its normal function. Whenever a Reset* signal is applied to the BS circuit, it also goes back to this state. One should also notice that whatever state the TAP controller is at, it will goes back to this state if 5 consecutive 1's are applied through TMS to the TAP controller.

Run-Test/Idle: This is a state at which the boundary scan circuitry is waiting for some test operations such as BIST operations to complete. One typical example is that if a BIST operation requires 2^{16} cycles to complete, then after setting up the initial condition for the BIST operation, the TAP controller will go back to this state and wait for 2^{16} cycles before it starts to shift out the test results.

Select-DR-Scan: This is a temporary state to allow the test data sequence for the selected test-data register to be initiated.

Capture-DR: In this state, data can be loaded in parallel to the data registers selected by the current instruction.

Shift-DR: In this state, test data are scanned in series through the data registers selected by the current instruction. The TAP controller may stay at this state as long as TMS=0. For each clock cycle, one data bit is shifted into (out of) the selected data register through TDI (TDO).

Exit-DR: All parallel-loaded (from the Capture-DR state) or shifted (from the Shift-DR state) data are held in the selected data register in this state.

Pause-DR: The BS pauses its function here to wait for some external operations. For example, when a long test data is to be loaded to the chip(s) under test, the external tester may need to reload the data from time to time.

Exit2-DR: This state represents the end of the Pause-DR operation, allows the TAP controller to go back to ShiftDR state for more data to shift in.

Update-DR: The test data stored in the first stage of boundary scan cells is loaded to the second stage in this state.

8. BYPASS REGISTER AND INSTRUCTION REGISTER

The Bypass Register is a 1-bit register, selected by the Bypass instruction and provides a basic serial-shift function.There is no parallel output (which means that the Update_DR control has no effect on the register), but there is a defined effect with the Capture_DR control - the register captures a hard-wired value of logic 0.

An Instruction register has a shift scan section that can be connected between TDI and TDO, and a hold section that holds the current instruction. There may be some decoding logic beyond the hold section depending on the width of the register and the number of different instructions.

The control signals to the Instruction register originate from the TAP controller and either cause a shift-in/shift-out through the Instruction register shift section, or cause the contents of the shift section to be passed across to the hold section (parallel Update operation).[4]

It is also possible to load (Capture) internal hard-wired values into the shift section of the Instruction register. The Instruction register must be at least two-bits long to allow coding of the four mandatory instructions - Extest, Bypass, Sample, Preload - but the maximum length of the Instruction register is not defined. In capture mode, the two least significant bits must capture a 01 pattern.[4]

9. INSTRUCTION SET

Standard describes four mandatory instructions: Extest, Bypass, Sample, and Preload, and six optional instructions: Intest, Idcode, Usercode, Runbist, Clamp and HighZ. Whenever a register is selected to become active between TDI and TDO, it is always possible to perform three operations on the register: parallel Capture followed by serial Shift followed by parallel Update. The order of these operations is fixed by the state-sequencing design of the TAP controller.[5]

10. BENEFITS OF BOUNDARY SCAN

The Designers often hesitate to use boundary-scan due to the additional silicon involved. But In many cases it may appear that the penalties outweigh the benefits for an ASIC. However, considering an analysis spanning all assembly levels and all test phases during the system's life, the benefits will usually outweigh the penalties.

The benefits provided by boundary-scan include the following:

lower test generation costs.
reduced test time.
reduced time to market.
simpler and less costly testers.
compatibility with tester interfaces.
high-density packaging devices accommodation.

11. CONCLUSION

Board level testing has become more complex with the increasing use of fine pitch, high pin count devices. and with the use of boundary scan the implementation of board level testing is done more efficiently and at lower cost. This standard provides a unique opportunity to simplify the design debug and test processes by enabling a simple and standard means of automatically creating and applying tests at the device, board, and system levels.

APPLICATIONS

-Low Cost Digital VLSI Testing circuits

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