DEVELOPMENT AND IMPLEMENTATION OF SPWM LOGIC USING DSPIC33FJ16GS402 FOR THREE PHASE INVERTER

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ABSTRACT: *Pulse Width Modulation (PWM) is a common technique used in many different applications of an inverter. This paper reported a pulse generation of SPWM technique for three phase inverter using dsPIC33FJ16GS402 controller. Logic for implementing SPWM technique is described here. The carrier frequency is designed for 20 kHz with varied modulation index (Ma) and the fundamental frequency is designed for 50 Hz. Phase-Locked Loop (PLL) logic is implemented. Simulation results of controller circuit, carried out in PROTEUS7.6 simulator are shown. An experimental result presented in this paper shows the effectiveness of pulse generation methodology.*

KEYWORDS: Inverter, SPWM, dsPIC, PLL, Modulation index (Ma).

1. INTRODUCTION

An inverter is a device that converts a direct current (dc) to alternating current (ac) at a desired output voltage or current and frequency. In order to function efficiently, an inverter controller is required. This is important so that an optimum inverter operation is achievable.

PWM is a common technique used in many different applications. This technique is the heart of the inverter system control signal. Up to now, many types of modulating modes have been brought forward in motion control and power conversion, such as classical VSI method, sinusoidal PWM(SPWM), space vector PWM(SVPWM),current tracking PWM, harmonic elimination PWM and so on [1]. These methods have some advantages and disadvantages, but the most widely techniques used are the sinusoidal PWM and the space vector PWM.

In a classical VSI (120^0,150^0, 180^0) method, the output voltage achieved is equal to a peak supply voltage [3]. Harmonics are also high. The lower order harmonics are present at nearer to fundamental one. Also the output rms voltage cannot be controlled (i.e. It remains constant not desired). It's a six step operation methodology.

To overcome this drawback, the modulation pulse methods are implemented [2]. Chopping the voltages and peak harmonics at switching frequency only are the achievements of modulation method. Advantages of this PWM method are as (1) reducing the total harmonic factor, (2) LOH is decreased, (3) variable rms output voltage (i.e. Output is controllable) is achieving.

Various types of inverters as well as controllers had been designed and implemented which vary from analogue and digital circuit controllers, signal processors, microcomputers, field programmable gate arrays (FPGAS) and digital signal processors (DSP). This paper presents a development and implementation of logic for generation of SPWM pulse using dsPIC type controller for three phase inverter.

Sine Wave Pulse Width Modulation (SPWM)

In this modulation method two signals are there. (1) Carrier signal: this signal is in triangular wave. The frequency of it is desired as per the frequency of switching. As the frequency is increases, the inverter switching frequency is increased. All the harmonics in line voltage with the order lower than (mf - 2) are eliminated. The harmonics are centred on mf and its multiples such as 2mf and 3mf. (2) Reference signal: it is in sign wave shape. The frequency of output voltage is depends on the frequency of reference signal. For 3 phases, three sine- waves with 120 degree apart from each other are required.

By appropriate passive filter the THD can be reduced up to 3 to 5% in SPWM, although the required dc link is higher than classical method. This method involves a comparison of the reference sine signal with a triangular carrier waveform and the detection of crossover instances to determine switching events.

The fundamental-frequency component in the inverter output voltage can be controlled by amplitude modulation index

$$Ma = \frac{Vm}{Vcr}$$

Where, Vm and Vcr are the peak values of the modulating and carrier waves respectively. Its amplitude is given by,

$$V_{ab1} = 0.866 * Ma * V_{dc}$$

The working principle of three phase inverter is explained in section two. The logic required to develop SPWM pulses are also explained in same section with selection table of dsPIC controller. Section three covers simulation and results of dsPIC using Proteus 7.6 software. All about hardware implementation and its experimental results are covered in last section.

2. IMPLEMENTED LOGIC USING DSPIC

Working Principle

Schematic diagram of three phase inverter is shown in figure1. DC supply used as an input of three phase inverter. Three phase inverter block consist a hex bridge with LC filter circuit. The ac output of inverter is given to the load. In control circuit dsPIC is used for SPWM gate pulse generation.

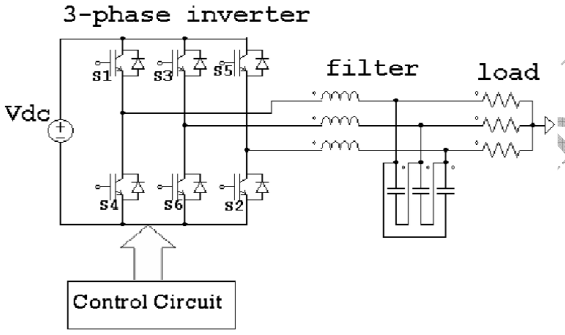

Fig.1 Schematic Diagram of three phase inverter

Development of Logic for SPWM Pulse Generation

Figure 2 shows the required SPWM pulse pattern for three phase inverter.

The reference waveform is the desired output waveform [5]. Whenever the voltage level of the sinusoidal waveform is higher than the triangular waveform, a logic '1' signal is generated. Otherwise, it is logic '0'. As a result, the controller produces SPWM gating signals to turn the switching devices on and off accordingly. Consequently, the inverter produces output voltage waveform resemble to the SPWM waveform. Then, the output voltages pass through the filter to removes higher harmonics from the waveform and make the waveform nearly sinusoidal.

The switching frequency of the SPWM signal is 20 kHz and the frequency of reference signal is 50Hz. So for the SPWM switching technique, total 400 PWM signal is generated. For each quarter cycle of the reference signal, 100 PWM signal is generated. The modulation index Ma can be controlled by varying an ADC cycle [6].

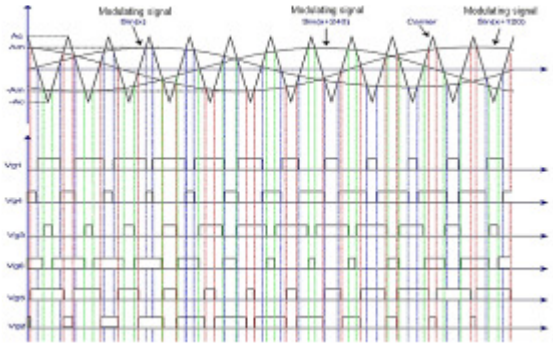

Fig.2 SPWM pulse pattern for three phase inverter

If we observe first 100 pulses which are held between 0 to 90 degree angles of reference wave, the duty cycle is increases. In same manner from 90 to 180 degree, it is decreasing. From 180 to 270, next 100 pulses are in form of decrementing. Once again they are in incrementing form in 270 to 360 degree. This cycle is repeated at 120 degree apart for second phase and for third phase it is situated at 240 degree. As we change the modulation index, the pulse width is changed.

Selection of DsPIC for Implementing SPWM Logic

TABLE I
DSPIC SELECTION TABLE

Product family	dsPIC 33FJ16 GS402	dsPIC 33FJ16MC304	dsPIC 33FJ32 GS606	dsPIC 33FJ32 MC304
Architecture	16	16	16	16
Program Memory	16KB	16KB	16KB	16KB
RAM	2048	2048	4096	4096
I/O Pins	21	35	53	35
Internal Oscillators	7.37 MHz	7.37MHz	7.37 MHz	7.37 MHz
CCP	2-std PWM	2-std PWM	2-std PWM	2-std PWM
MC PWM Ch.	6	8	12	8
SMPS PWM Ch.	6		12	
Timers	3x16 bit,1x32 bit	3x16bit, 1x32 bit	5x16 bit,	5x16bit, 2x32 bit

dsPIC controller consists some futures: (1)three 16 bit timers,(2)10 bit ADC,(3)PLL logic for increases resolution,(4)immediate update in duty cycle,(5) dead band logic between complimentary pulses. DsPIC33FJ16GS402 is selected on the basis of following table. This controller's type is 16 bit RAM, general SMPS application with 28 pin and 6 SMPS PWM channels [4].

3. SIMULATION RESULT

Simulation of control circuit

The pulse pattern as per discussion is simulated through dsPIC33FJ16MC304. Proteus7.6 (simulation software), MPLab8.46 (programming software), HTC-Compiler software are used for this simulation as per figure 3.

The step of programming for SPWM generation logic is as following:

(i)Disable the PWM pin (PxTCON) output drivers as an input by setting the associated TRIS bit.

(ii) Set the PWM period by loading the TxTPER register.

(iii) Configure the CCP module for the PWM mode by loading the PWMxCONy register with the appropriate values.

(iv) Set the PWM duty cycle by loading the PxDCy register.

(v)Set the dead time by loading the PxDTCONy register.

(vi) Configure and start Timer2

(vii)Enable the PWMx pin output driver by clearing the associated TRIS bit.

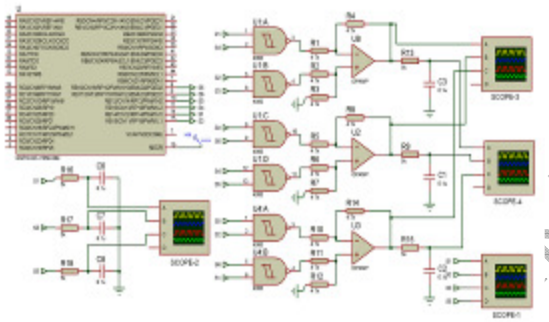

Fig.3 Simulation diagram of SPWM gate pulse generation circuit

Various simulation results are as shown in figure 4. Three gate pulses of upper switches of each leg are as shown in figure4 (a).

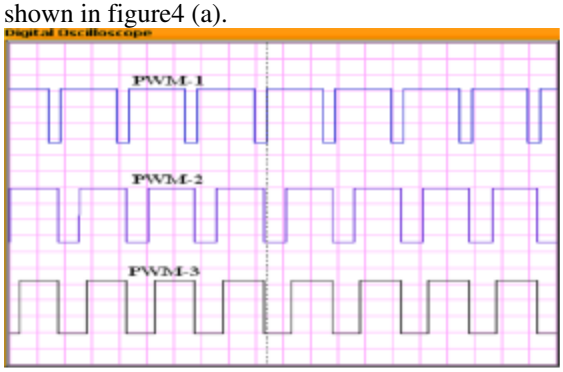

Fig.4(a) Generated gate pulses for three upper switches. (Scale: x-axis:20usec/div, y-axis:1V/div)

400 pulses of first upper switch with related pole waveform are shown in figure 4(b). Dead band with 2usectime between to complimentary gate pulse is achieved by dead band register of dsPIC as per figure4 (c).

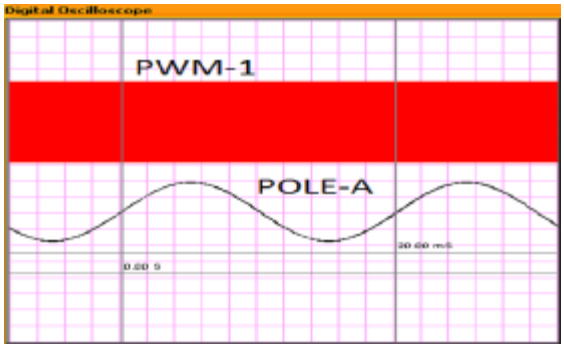

Fig. 4(b) 400 pulses of first upper switch with related pole waveform. (scale: x-axis:2msec/div, y-axis:1v/div)

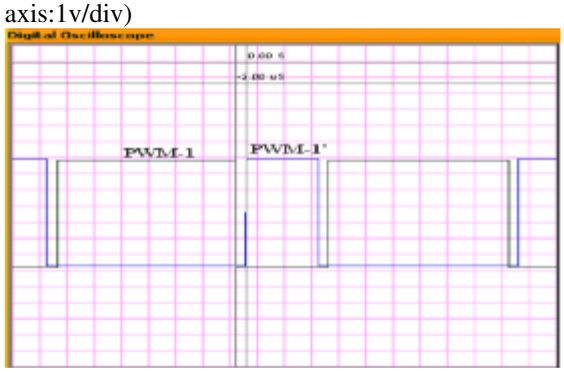

Fig.4(c) Two complimentary pulse of leg 1 with dead band. (Scale: x-axis: 5usec/div, y-axis: 0.75V/div)

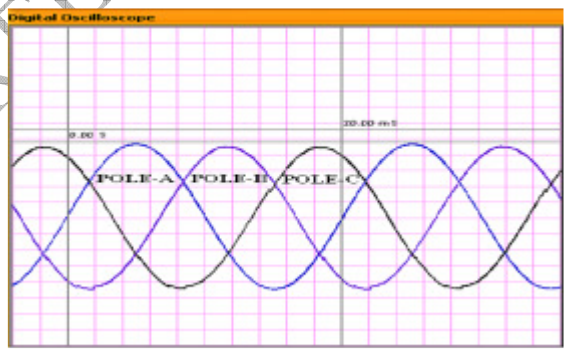

Fig.4(d) Output of three pulses with RC low-pass filter with higher modulation index. (Scale: x-axis: 2msec/div, y-axis: 1V/div)

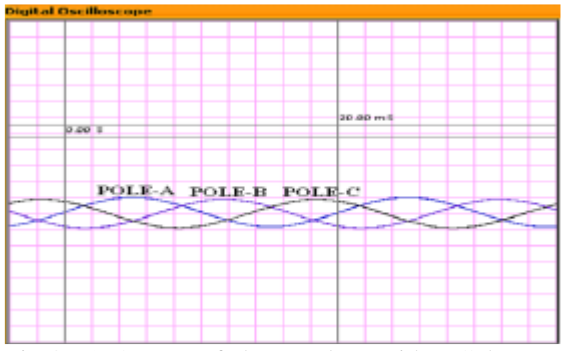

Fig.4 (e) Output of three pulses with RC low-pass filter with lower modulation index. (Scale: x-axis: 2msec/div, y-axis: 1V/div)

For seen the 120degree apartness between 3 leg, RC low pass filter is simulated at output of three

generated pulses gives a sinusoidal output as per figure 4(d).Figure 4(e) shows the RC output with less modulating index logic.

Testing of Control Card Logic

The control card is developed by using IC dsPIC33FJ16GS402. Six pulses as outputs of this IC are generated as SPWM logic. Now it is required to check the effectiveness of this logic. For that a testing logic is used in simulation as well as hardware side to check the pole voltage at the output side of control card. Output of control IC is given to the testing components. IC 4093 and LM324 are used for logic testing. The output of this circuit gives pole voltage across each pole using IC 4093. LM324 gives the line voltage across each line. For more accurate checking, again RC network is simulated at the end of line voltage output. Figure4 (f) shows the line voltages Vab, Vbc and Vca. Each voltage is 120 degree apart from one another. It indicates that pulses are working as SPWM logic. The pulse voltage is 5 Volt, so it produces the same level at output side. Figure4 (f) indicates accurateness of the logic.

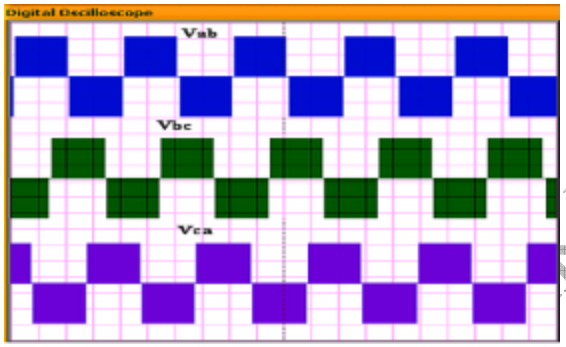

Fig.4(f) Line to line inverter output voltage waveforms. (Scale: x-axis: 5msec/div, y-axis: 2V/div)

4. HARDWARE IMPLEMENTATION OF DSPIC CONTROLLER

Controller circuit block consist a dsPIC33FJ16GS402. It is a 28 pin IC, operated at 3.3 Volt supply. The schematic diagram of developed controller card is shown in figure 5(a). Pin 2 is used for changing modulation index on the basis of changing of operated voltage for open loop condition. Output gate pulses are getting from pin 21-26. RC logic is also implemented in this card to achieving three phase pole voltage.

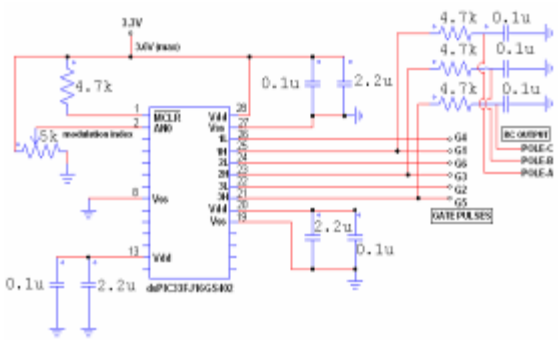

Fig.5(a) Schematic diagram of developed controlling circuit.

Figure 5(b) shows flow chart of dsPIC33FJ16GS402 for SPWM logic which is implemented for six gate pulse generation of three phase inverter.

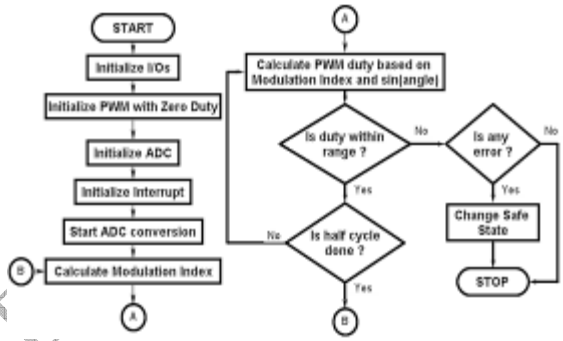

Fig.5 (b) Flow chart for SPWM technique.

PLL Logic Implementation

$$F_{OSC} = F_{IN} * (M/N1 * N2)$$

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation [4]. The PLL provides significant flexibility in selecting the device operating speed. The output of the primary oscillator or FRC, denoted as FIN, is divided down by a pre scale factor (N1) of 2, 3 ... or 33 before being provided to the PLLs Voltage Controlled Oscillator (VCO). The input to the VCO must be selected in the range of 0.8 MHz to 8 MHz. The pre scale factor N1 is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>). The PLL Feedback Divisor, selected using the PLLDIV<8:0> bits (PLLFBD<8:0>), provides a factor, M, by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz. The VCO output is further divided by a post scale factor, N2. This factor is selected using the PLLPOST <1:0> bits (CLKDIV<7:6>). N2 can be 2, 4, or 8, and must be selected such that the PLL output frequency (FOSC) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS. For a primary oscillator or FRC oscillator, output FIN, the PLL output FOSC is as per equation.FIN is 7.8 MHz here. If PLLPRE<4:0> = 0, then N1 = 2. This yields a VCO input of 7.8/2 ≈ 5

MHz, which is within the acceptable range of 0.8-8 MHz. If PLLDIV<8:0> = 0x1E, then M = 32. This yields a VCO output of 5 x 32 = 160 MHz, which is within the 100-200 MHz ranged needed. If PLLPOST<1:0> = 0, then N2 = 2. This provides a Fosc of 160/2 = 80 MHz. The resultant device operating speed is 80/2 = 40 MIPS.

Hardware Results

The photo view of developed card is shown in figure 5(c). Regulator unit gives required 3.3 Volts to control unit. Pin 21 to pin 26 of control unit gives required six SPWM pulses. Three upper pulses are connected to R.C unit. It is used to check the 120 degree apartness between three legs at any time of testing.

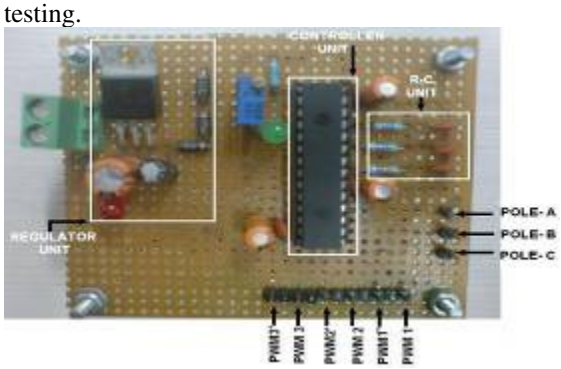

Fig.5(c) Photo view of developed card.

Various hardware results of SPWM generation circuit using dsPIC33FJ16GS402 are shown here. Generated gate pulses for three upper switches are shown in figure 6(a) for 20 kHz frequency. These pulses are 120 degree apart from each.

Fig.6(a) Generated gate pulses for three upper switches. (Scale: x-axis:25usec/div, y-axis:2V/div)

400 pulses of first upper switch with related pole waveform are shown in figure 6(b).PWM-1 and PWM-1' are generated using complement as well as dead band logic which can be implemented using dead band register in dsPIC. Two complimentary pulse of leg 1 with dead band of 2microsecond are shown in figure 6(c). For checking modulation index, RC low pass filter circuit is used in hardware. Output of three pulses with RC low-pass filter with different modulation indexes are shown in figure 6(d)-6(e).

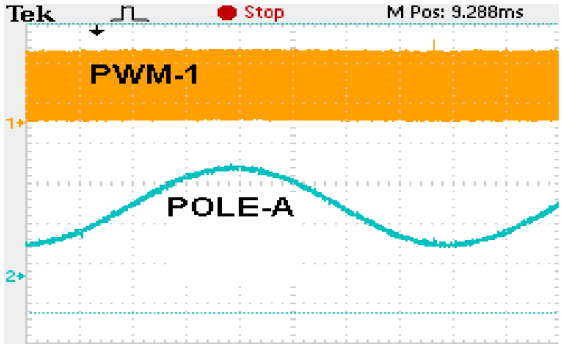

Fig.6(b) 400 pulses of first upper switch with related pole waveform. (Scale: x-axis:2.5msec/div, y-axis:1V/div)

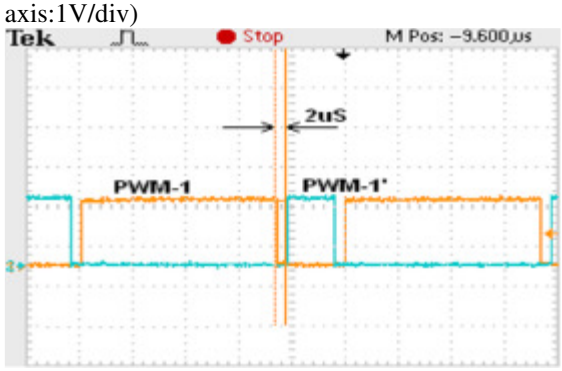

Fig.6(c) Two complimentary pulse of leg 1 with dead band. (Scale: x-axis: 10usec/div, y-axis: 2V/div)

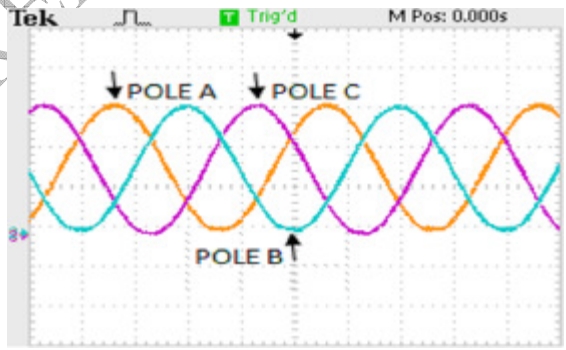

Fig.6(d) Output of three pulses with RC low-pass filter. (Scale: x-axis: 5msec/div, y-axis: 1V/div)

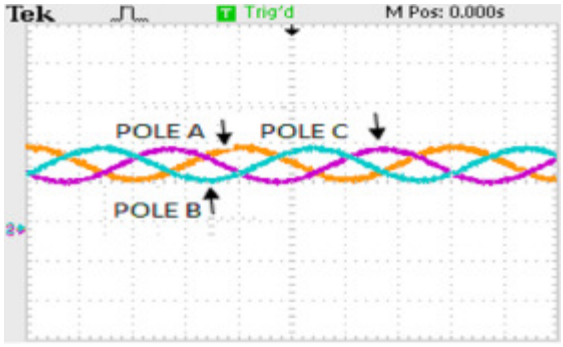

Fig.6(e) Output of three pulses with RC low-pass filter. (Scale: x-axis: 5msec/div, y-axis: 1V/div)

Figure 6(f) shows the line voltages Vab, Vbc and Vca. Each voltage is 120 degree apart from one another. It indicates that pulses are working as SPWM logic.

The pulse voltage is 5 Volt, so it produces the same level at output side. It indicates accurateness of the logic.

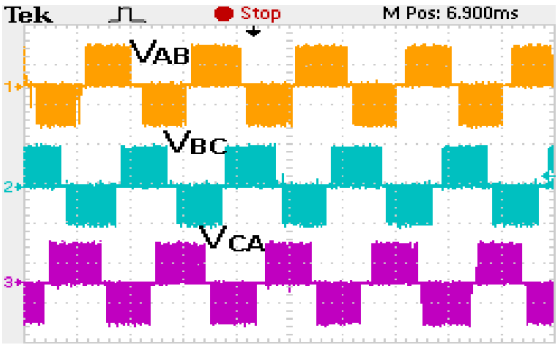

Fig.6(f) Line to line inverter output voltage waveforms. (Scale: x-axis: 25msec/div, y-axis: 5V/div)

5. CONCLUSION

SPWM generating technique is mostly used in three phase inverter system. Various logics like compliment pulse, dead band, varying duty cycle can be implemented in dsPIC controller by setting of proper available registers. Nearer to 40 MIPS speed of controller is obtained by the given PLL logic. All six pulses of 3.3volts are obtained. By applying the same logic hardware is also developed. Modulation logic is also checked from range of 0 to 3.3 volts for 0 to 0.96 modulation index with ADC interfacing. Generated pulses are implemented in hex bridge IGBT based power module. Close loop controlling will be also implemented in future in the same.

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