DESIGN SYSTEM ON CHIP FOR VIDEO COMPRESSION

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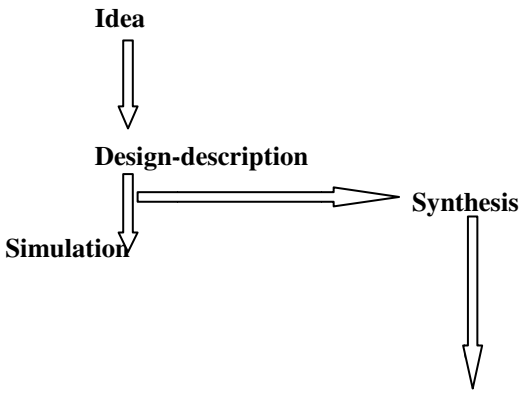
ABSTRACT:*In this paper we use FPGA as a system on chip which is then use for video compression by discrete cosine transform respectively. A key step in the design flow is emulation. The hardware is mapped onto an emulation platform based on a field programmable gate array (FPGA) that mimics the behavior of SOC. Implementing SOC such as gap between modeling & implementation generally system modals are written in C, but system implementation are in hardware description languages (HDL) i.e. video compression using system on chip using very hardware description language.finly soc built on FPGA using Xilinx software, because field programmable gate array spatially support this language, also consumes low power, high speed performance Video compression is reducing redundancy in video data Compression technique used in Videoconferencing, Video telephony, Video on Internet, HDTV broadcast UHDTV ,digital video broadcasting etc*

KEYWORDS: Video Compression, SOC, MPEG, Discrete Cosine Transforms, VHDL

1. INTRODUCTIN

System on chip refers to integrating all componenent of an electronic into single integrating circuits. Application of soc is field of digital, analog, mixed-signal & various fields.[1] A typical application is in area of embedded system. Embedded system is a special-purpose computer system designed to perform one or few dedicated task with real-time computing constraints.[6] for proper, reliable, controlled, and timely operation some suitable real time operating system is used. By video scalar/Compressor we convert video of one resolution & aspect ratio to another resolution, of our requirements as minimum 25 frames/second as per PAL rule and 30 frames/second as per NTSC standard rule. For video compression as a perspiration of vision, then that scaled video given to a specific processor to put into motion jpeg which is transmitted via Ethernet connection & finely this all components built on system on chip. Many formats are available for video compression some of them .are in binary, we can say that which give video data into bit-stream or binary form, because VHDL only works on binary data. So video or moving picture is first converted into digital after than encoding data are dump into FPGA i.e. our system on chip. Available (lossy or lossless compression system) video compression formats are MPEG-2 Part 2, MPEG-4 Part-2, H.264(MPEG-4 Part 10), Theora, Dirac Real Video and VP8.etc…

2. PROPOSED FLOW OF WORK



3. BASIC STEPS FOR VIDEO COMRESSION

1. Take I/P video of our choice e.g. (as minimum 25 frames/second as or PAL rule and 30 frames/second as per NTSC standard rule)

2. Read it bitwise from register buffer & then select pixel from matrix. (As shown in fig.1) simulation result shown fig.no.2

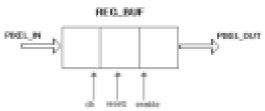


Fig.1 Register-buffer

3. Compress data of video using DCT

4. O/P of our requirements, in compressed form

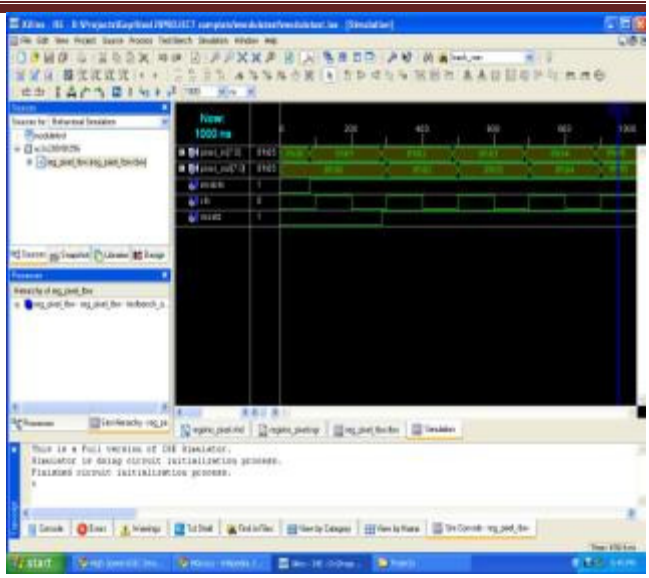


Fig.2 Simulation result

4. TYPES OF COMPRESSION SYSTEM:

There are two types of compression systems are available and they are Lossy & Lossless video compression system respectively

Lossy compression: It is used when requirements of higher compression ratio like, Motion photographic expert Group

Lossless video compression: Lossless compression system- which aim at minimizing the bit rate of compressed o/p without any distortion of video

5. FORMAT USED FOR VIDEO COMPRESSION

M-JPEG is frequently used in non-linear video editing systems Modern desktop CPUs are powerful enough to work with high-definition video, across the wide variation in graphics and operating-systems in use. Because it is a mature format, needs no special hardware on modern PCs, and natively offers random-access to any frame, M-JPEG support is widespread in video-capture and editing equipment. Motion JPEG uses a lossy form of intraframe compression based on the discrete cosine transform (DCT). This mathematical operation converts each frame/field of the video source from the spatial (2D) domain into the frequency domain In the transform domain, the process of reducing information is called quantization.

Coefficients, which contribute less to the over picture than other coefficients, are characteristically small-values with high compressibility. The quantized coefficients are then sequenced and lossless packed into the output bit stream. Nearly all software implementations of M-JPEG permit control over the compression-ratio [7].

[A] The three major picture types used in the different video algorithms are **I**, **P** and **B**. They are different in the following characteristics:

I frames are the least compressible but don't require other video frames to decode.

P-frames can use data from previous frames to decompress and are more compressible than I frames.

B-frames can use both previous and forward frames for data reference to get the highest amount of data compression.

.[B] Frame segmentation: Actual frame is divided into macro block (8*8) or (16*16) pixels. MPEG uses (16*16) pixel [7]

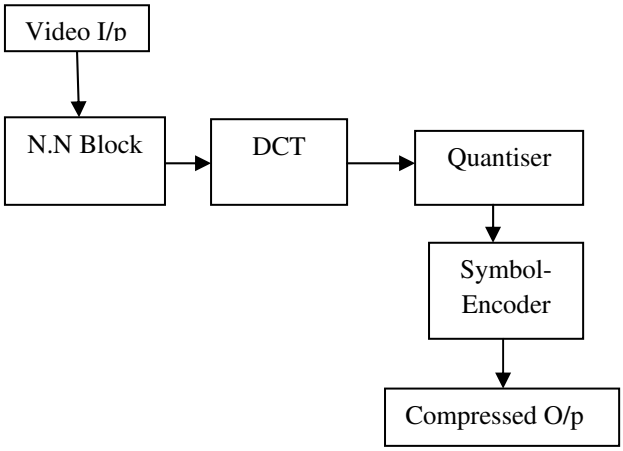
[C] Search Threshold: in order to minimize no. of motion estimation calculation, they are only calculated if difference between two blocks at same position is higher than threshold; other whole block is transmitted [7].

[D**]** Block-matching: stitch together actual predicted frames by using blocks from previous frames

[E] Error prediction**:** Original frames are compared and differences are coded due to this less data needed to be store.

[F] Peak signal to noise ratio (PSNR): It is the ratio between the maximum possible power of a signal and power of corrupting noise. PSNR is given in logarithmic decibel scale

6. APPLYING DCT FOR TRANSFORMATION & QUANTIZATION



7. PROPOSED DCT ALGORITHM:

1. Video is a sequence of frames, so separately each frame is broken into (16*16) blocks of pixels.

2. Working from left to right, top to bottom DCT applied to each block [3].

3. Each block is compressed through quantizing. (If more zeros occurs after quantizing means compression is too high). [3,5].

4 By, entropy-encoding coefficient of quantized matrix is converted into binary data (100101110101….).Then binary stream is burn or dump into FPGA kit which acts as a SOC.

8. CONCLUSION

Video-compression is reducing redundancy in video data Compression technique. Also allows more efficient storage & transmission of data. By using DCT computation perform a large number of multiplication & addition but with well established and regular data access pattern.[5]. Generally system modals are written in C, but system implementation are in hardware description languages (HDL) & code then dump on soc to make system fast for giving simulation & other result.[1] In this we use MPEG which is robust.

RRFRANCES

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