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COUPLED INDUCTOR BASED SOFT SWITCHED INTERLEAVED HIGH STEP UP DC-DC CONVERTER

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***Abstract*— For PV fed applications, higher input current ripple leads to reduced life of the system. Hence interleaved DC-DC converter topologies have been developed.**
The proposed ZVS topology has three stages namely Interleaved, Coupled Inductor (CI) and Diode Capacitor Multiplier (DCM). First stage reduces the input current ripple, CI stage enhances power handling capability of the converter and the DCM cells are connected to obtain higher voltage gain. Since high voltage gain is obtained through DCM cells and the turns ratio of the CI, the voltage stress on the main power switches is only a fraction of the output voltage.

The proposed ZVS based DC-DC converter with high step up capability has been designed and simulated in MATLAB / Simulink environment.

Keywords—interleaved,coupledinductor,current ripple,zvs,matlab,

I. INTRODUCTION

The growing use of renewable energy sources (RESs) and Energy storage systems (ESS), due to global environmental concern, brings new challenges to the energy conversion technology. Because some devices that store or produce electrical energy (e.g., batteries, ultra-capacitors, fuel cells and solar photovoltaic) is often realized using multiple low voltage cells, which are usually connected in series to produce sufficient voltages for the intended application. Unfortunately, series connection of cells degrades the system performance, adds complexity to the system, and possible temperature rise due to fabrication variation and different operating conditions between cells. In batteries, this may be related to the state of charge of a cell. In solar arrays, it may be due to a change in solar irradiance or partial shading of the array.

The boost and buck-boost converters are the simplest non-isolation topologies that produce an output voltage that is greater in magnitude than the source voltage. However, the conventional boost and buck-boost converters must operate at extreme duty ratio to achieve high voltage gain (in particular ten times). This is an undesirable operating point.

Since the output diode sustains short pulse, high amplitude, current pulses which result in severe reverse recovery losses. Besides, as the output voltage increases so must the voltage rating of the semiconductor switching devices and at high duty ratio the conduction losses of the semiconductor device can make a more significant impact to the performance of the system. Furthermore, as the duty ratio approaches unity, the output voltage approaches zero, and the efficiency decreases to zero. Consequently, the converter may suffer poor dynamic response to system parameter changes and potential load variations. This behaviour is typical of converters having boost or buck-boost characteristics. The challenge for any high step-up DC-DC converter is to avoid extreme duty ratio operation.

Some of the major shortcomings of extreme duty ratio operation include reverse recovery loss of the output diode as a result of short pulse current with large amplitude. Furthermore, the output diode reverse recovery problem can lead to higher turn-on switching loss for the power switch. For this reason, there is considerable motivation to improve the performance of high step-up boost converters by alleviating the diode reverse recovery loss so that switching loss can be significantly reduced. Literature has revealed that the power device voltage rating in conventional boost converter is the same as the converter output voltage. Another concern related to the efficiency of high step-up converters is power device rating.

A high voltage rated device is not a good choice for the steady state operation because of the high input current (as the power MOSFET rating increases, so does the on-state resistance Rds_on resulting in conduction losses which also degrade the efficiency). The challenge for a high step-up converter is to dramatically reduce the conduction losses. Appropriate duty ratio operation, conduction losses reduction and alleviation of diode reverse recovery problem can greatly improve the efficiency of power conversion. It is the aim of this thesis to investigate methods of improving the performance of high step-up converters.

Various techniques for high step-up conversion have been reported in the literature Depending on the application, they are either isolated or non-isolated topologies. Transformer based converters can easily achieve high voltage gain by adjusting the turns ratio and utilises low rated devices to reduce the conduction losses. However, the leakage inductor induces high voltage stress to the power device and traditionally requires a snubber. Either RCD snubber circuit or a clamp circuit must be used to handle the leakage energy.

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II. NOVEL TECHNIQUES OF DC-DC BOOST CONVERTER

A.General Structure of DC-DC Boost Converters

Depending on the configuration, the input side can be current fed or voltage fed. The input voltage can be a battery, fuel cell or solar photovoltaic

B. Isolated DC-DC Boost Converters

The high-frequency transformer based system is an attractive solution for providing galvanic isolation and impedance matching between the source and load. As an example, isolation is usually required by regulatory agencies in off-line power supply applications. Classical converters with galvanic isolation such as flyback, current-fed push-pull converters can easily achieve high voltage gain by adjusting the turns ratio. However from an efficiency standpoint, the high-frequency transformer implies additional cost, losses and inhibits developing a compact converter. Thus, the volume weight and losses are the main limitations of isolated converters in embedded applications. Isolated boost converters are either current-fed or voltage-fed. Some typical examples of isolated DC-DC converters topologies include flyback, forward, full bridge, half bridge, push-pull converters or their variations.

C. Non-isolated DC- DC Boost Converter

Rather than the isolated converters, non-isolated DC-DC converters can be used to improve the efficiency. Consequently, the volume, weight and losses associated with the high-frequency transformer are reduced. Furthermore, in the high power application where weight size is the main concern, the transformer-less structure is the most attractive. It is becoming a more suitable solution to employ non-isolated converters to reduce the system cost and improve the efficiency. Since the passive components size and weight of non-isolated converters vary inversely with frequency, the components then operate at converter switching frequency in tens of kilohertz (KHz) range or higher. This high frequency leads to dramatic reduction in converter size and weight. In summary, for applications that require isolation between source and load based on safety measures, the isolated topologies are the right choices. However, in high power applications where volume weight is the main concern, the non-isolated topologies are the best option. The basic non-isolated DC-DC step-up topologies that produce an output voltage higher in magnitude than the input voltage are the boost and buck-boost converters.

D.Limitations of Conventional Converters in High step-up Applications

The boost and buck-boost converters are the simplest PWM controlled topologies for voltage step-up. However, these converters typically operate under extreme duty ratio to achieve high voltage gain. As a consequence, significant voltage and current stresses are incurred by the power converter devices and poor dynamic characteristics can result in the controlled output response. Besides, the power device rating is proportional to the output voltage and a high rated power device potentially increases the conduction losses which also degrade the efficiency. Furthermore, the output diodes often sustain short, but high amplitude, current pulses due to the narrow turn off time; which induces reverse recovery losses.

During the switch turn on instant, the diode DO is reversed biased, and the input source charges the inductor L. When the switch turns off, the load receives energy from the input as well as the inductor. The capacitor CO removes the switching harmonics from the applied input signal. Noticeably, the energy transfer in a step-up (boost) converter is between a voltage and current source. Since in a steady state, the capacitor or inductor can be represented by their instantaneous voltage or currents as an equivalent voltage and current sources respectively.

E.Zero Voltage Switching (ZVS) Technique The objective of the technique is to use resonance to force the voltage across the device to zero prior to its turn-on or turn-off. A (ZVS) turn-on is implemented by discharging the parasitic capacitor and subsequently forcing the antiparallel diode of the device to conduct prior to the application of the gate signal. Therefore, the switch turns-on with only antiparallel diode voltage drop. A (ZVS) turn-off is achieved sometimes by adding a capacitor across the switch to limits the overlap between the voltage and current during turn-off. If the switch voltage waveform is shaped during turn-on and turn-off period (i.e. switching transition) to create a (ZVS) condition, such phenomenon is called zero voltage transition (ZVT). MOSFET is used in a medium power, suitable for high switching frequency applications and have significant drain source capacitance; they are mostly used in (ZVS) circuits. An external snubber capacitor is often added to drain-source capacitance to ensure (ZVS) turn-off. To ensure (ZVS) turn-on of the device a negative current usually discharges the snubber capacitor and makes the antiparallel diode conduct so that the device can turn-on with (ZVS) condition.

F..*Zero Current Switching (ZCS) Technique*

(ZCS) is another technique similar to (ZVS) that uses resonance to force the current following through the switch to zero during turn-on or off. A (ZCS) turn-on is implemented by including a small inductor in series with the switch that controls the rise of the current when the switch turn-on. During turn-on, the switch current increases linearly from zero. Finally, the switch can be commutated at the next zero current duration. Likewise, if the switch current waveform is shaped during turn-on and turn-off period (i.e. switching transition) to create a (ZCS) condition, such phenomenon is called zero current transition (ZCT). The major drawback of MOSFET when used to implement (ZCS) is the capacitive turn-on losses and high current stress. IGBT is a minority carrier device, have large tail current in the turn-off process. Thus, (ZCS) are useful particularly in minimizing the switching loss for power

III. PROPOSED CONVERTER AND OPERATING PRINCIPLE

A two phase interleaved boost converter (IBC) is considered as the fundamental topology. Figure represents a CI based interleaved topology in which one of the phases of conventional IBC is left unchanged while the boost inductor is replaced by a CI in the other phase. Resultantly, the primary inductance of the CI acts as the energy storage and energy transfer inductor. The secondary of this CI is suitably connected to output capacitor (C02 in this case). The net output voltage is obtained across the series combination of output capacitors C01 and C02. Thus, the overall voltage gain contribution is due to two stages – the interleaved boost stage and the CI stage. By intuition, it can be realized that the overall voltage gain of this converter shall be higher than the conventional IBC due to CI with a turns ratio more than 1.

Power circuit of CI based IBC.

To enhance the voltage gain and power handling capability, DCMs are judiciously added to CI based topology. Now, the three stages present are recognized as (i) interleaved stage, (ii) DCM stage and (iii) CI stage. Each stage has its own prominent feature as listed below:

1) Interleaved stage aids in reducing the input current ripple.

2)DCM stage provides high voltage gain with reduces number of components compared to VMC stages, thereby reducing circuit complexity and voltage stress on the main switch.

3) CI stage helps to enhance the voltage gain and handle higher power.

The voltage gain of the presented converter now depends on (i) turns-ratio of the CI (T) and (ii) number of DCMs used (N). This provides added flexibility to the user in terms of meeting the voltage gain requirement.

Extension of this concept leads to a generalized converter structure. The converter structure has an interleaved converter with P phases using Q number of coupled inductors (Q ≤ P), each with T turns ratio. It must be noted that N number of DCM stages can also be added appropriately. The load is connected across the series combination of output capacitors.

The proposed CI based soft-switched interleaved high gain DC-DC converter. The circuit has two switches which are operated at 180 phase shift with a duty cycle of D. Diodes DS1 and DS2 are the intrinsic body diodes of S1 and S2 respectively. CS1 and CS2 are the resonating capacitors which have been added across the switches so as to undergo resonance with the inductors L1 and L21 in order to achieve ZVS turn ON of the switches.

The diode-capacitor pair D1-C1 forms the 1st DCM cell. Similarly, the remaining DCM cells are obtained from D2-C2 through D5-C5. Diode D6 acts as the output diode while capacitors C01 and C02 serve as the output capacitors of CI and DCM stagesThus, a CI based soft-switched interleaved DC-DC converter containing 5 DCM cells is developed.

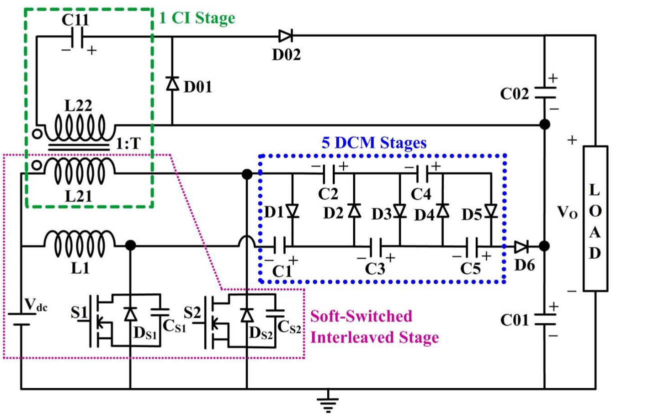

Fig.1.Proposed converter circuit

IV. SIMULATION RESULTS

TABLE 1. PROTOTYPE SPECIFICATIONS OF SIMULATION COMPONENTS

Parameter	Symbol	Rating
Input voltage	Vin	20V
Output voltage	Vo	360V
Output power	Po	200W
Switching frequency	fs	50kHz
Inductor	L1, L21	100mH
Turn ratio of CI	T	3
Number of DCM	N	5
Capacitors	C1 – C5	10mF/250V – Electrolytic
Output capacitor	C01, C02	47mF/500V – Electrolytic
Resonant capacitors	CS1, CS2	47nF/600V – Polystyrene
Switches	S1, S2	FDPF33N25T(250V/33A)
Diodes	D1 – D6	MUR1660 (600V/16A)
Diodes	D01, D02	1N5408

CONVENTIONAL CIRCUIT:

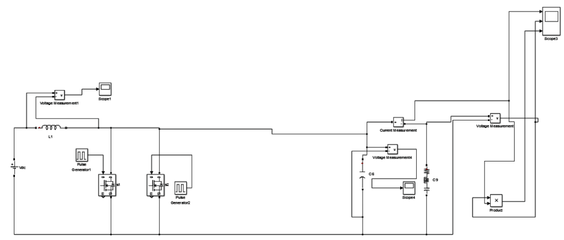

Fig 2.Simulation Model Of Conventional Circuit

PROPOSED CONVERTER CIRCUIT:

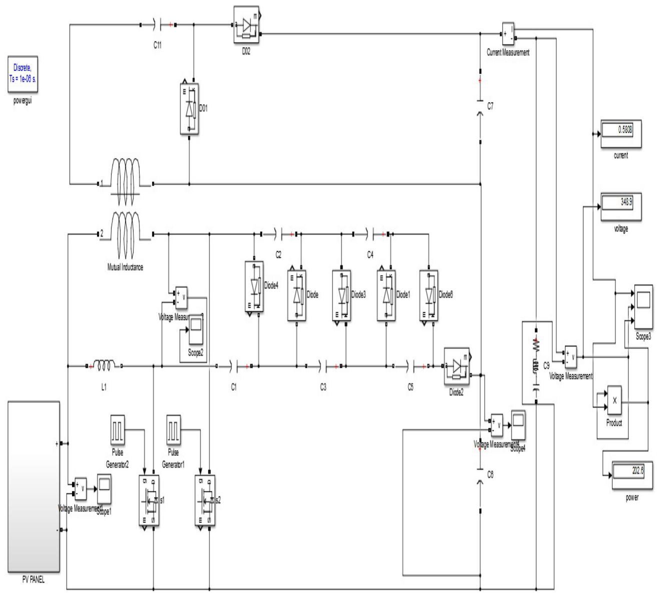

Fig.3.Simulation model of proposed converter

SIMULATION WAVEFORMS:

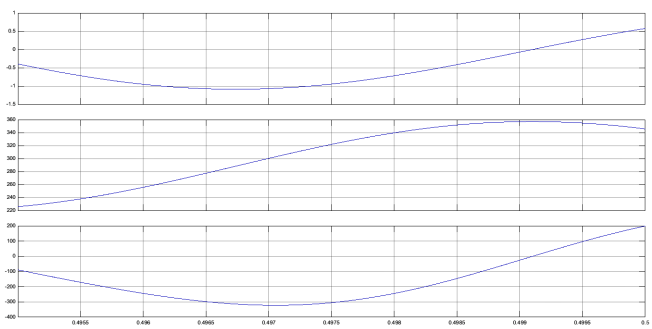

Fig.4.output current,output voltage and output power

The output voltage obtained from the simulation model of the interleaved boost converter circuit is 360V and the output power obtained from the Simulink model is 200W.

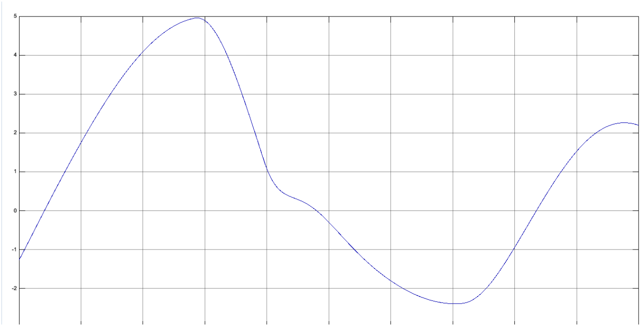

Fig.5.output at the interleaving stage

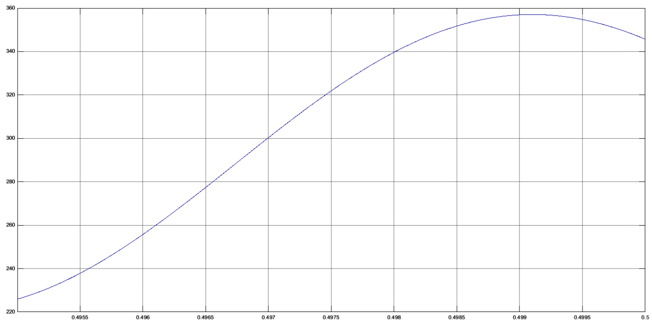

Fig.6 .Output voltage measured on proposed converter circuit.

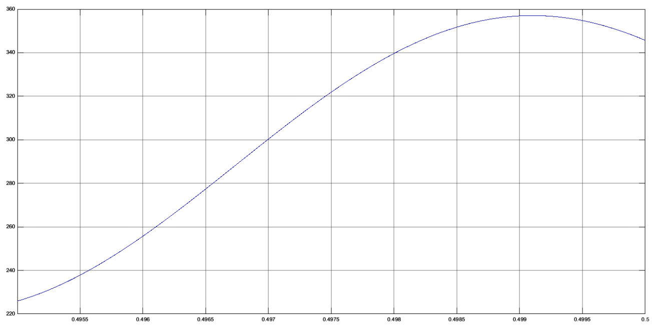

Fig.7.Output voltage measured on conventional circuit.

The output at the interleaving stage is obtained to be sinusoidal waveform.As the input is dc voltage and a sinusoidal output is obtained from the interleaved stage.

The output voltage measured on conventional circuit is 55V.The output voltage measured in proposed converter circuit is 354V.

CONCLUSION

A CI based soft-switched interleaved high gain DCDC converter which provides a high voltage conversion ratio has been developed, analysed, designed and practically demonstrated. By using 5 DCMs, 1 CI with a turns-ratio of 3 and operating the switches at 0.5 duty ratio, a voltage gain of 18 was obtained. Since DCMs were used as gain extension stages to enhance the overall voltage gain of the converter, both the switches and all the diodes experienced a very low voltage stress which was just a fraction of the output voltage. The operating efficiency of the converter was improved by employing ZVS technique. The converter operated at a full load efficiency of 95% while delivering 200W of power to the output. This topology is suitable for photovoltaic applications as the input current ripple is almost zero due to interleaving concept.

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